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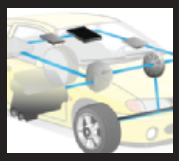

TIMING IS EVERYTHING IN SOC DESIGN

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USER-FRIENDLY MODEL SIMPLIFIES SPICE OP-AMP SIMULATION

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CONNECTING SYSTEMS TO DISPLAYS:

WHAT WE GOT HERE IS FAILURE TO COMMUNICATE

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Ultimate Precision. Low Power. Small Size.

Amplifiers Use TI's New 36V Bipolar SiGe Process

Device	Input	V_N	V_{OS}	GBW	I_Q	V_S	Package
OPA211	Bipolar	$1nV/\sqrt{Hz}$	100µV	80MHz	3.5mA	±18V	MSOP-8
OPA827	JFET	$4.5nV/\sqrt{Hz}$	250µV	18MHz	4.2mA	±18V	MSOP-8

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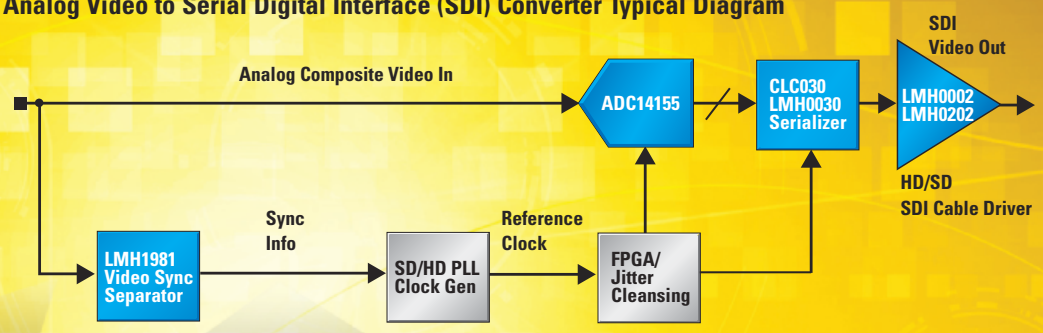
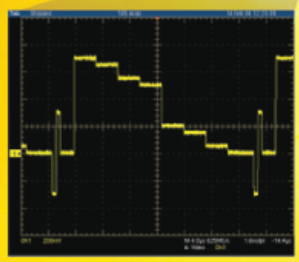
Ultra Low-Jitter Sync Separator for SD/HD Video

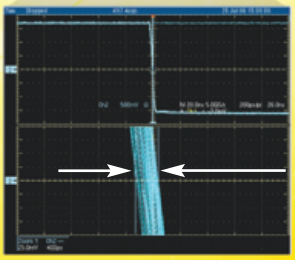
New LMH1981 Features 50% Sync Slicing for Precise Output Timing

Analog Video to Serial Digital Interface (SDI) Converter Typical Diagram





720p/60 Tri-Level Input



720p/60 H-Sync Output

LMH1981 in TSSOP-14 packaging
Shown at actual size 4.40 x 5.00 x 0.90 mm

AVAILABLE LEAD-FREE

LMH1981 Features

- 50% sync slicing
- Low-jitter horizontal sync outputs
- Supports NTSC, PAL, SECAM, 480i, 480p, 576i, 576p, 720p, 1080i, and 1080p
- Accepts video sync signals from 140 mV_{P-P} to 1.2 V_{P-P}
- No external programming with µC required
- Horizontal sync output propagation delay <50 ns
- 3.3V or 5V single supply operation

LMH1981 Outputs

- Horizontal sync
- Vertical sync
- Odd/Even field
- Burst/back porch clamp
- Composite sync
- Video format (horizontal lines/field)

Ideal for use in sync separation, A/V clock generation, video genlock, back porch clamp generator, video format detection circuit, and analog-to-SDI converter applications

For FREE samples, datasheets, online design tools, and more information on the LMH1981, contact us today at
amplifiers.national.com
Or call 1-800-272-9959

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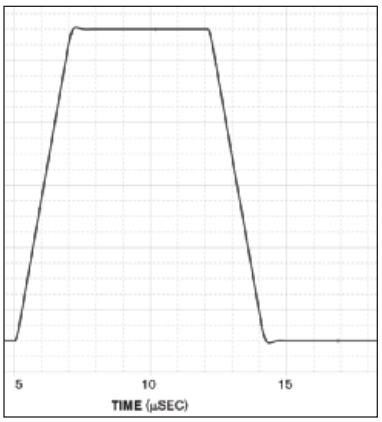


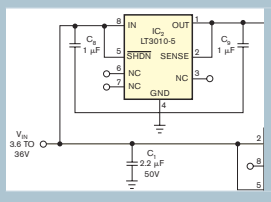
CONNECTING SYSTEMS TO DISPLAYS:

What we got here is failure to communicate

Timing is everything in SOC design

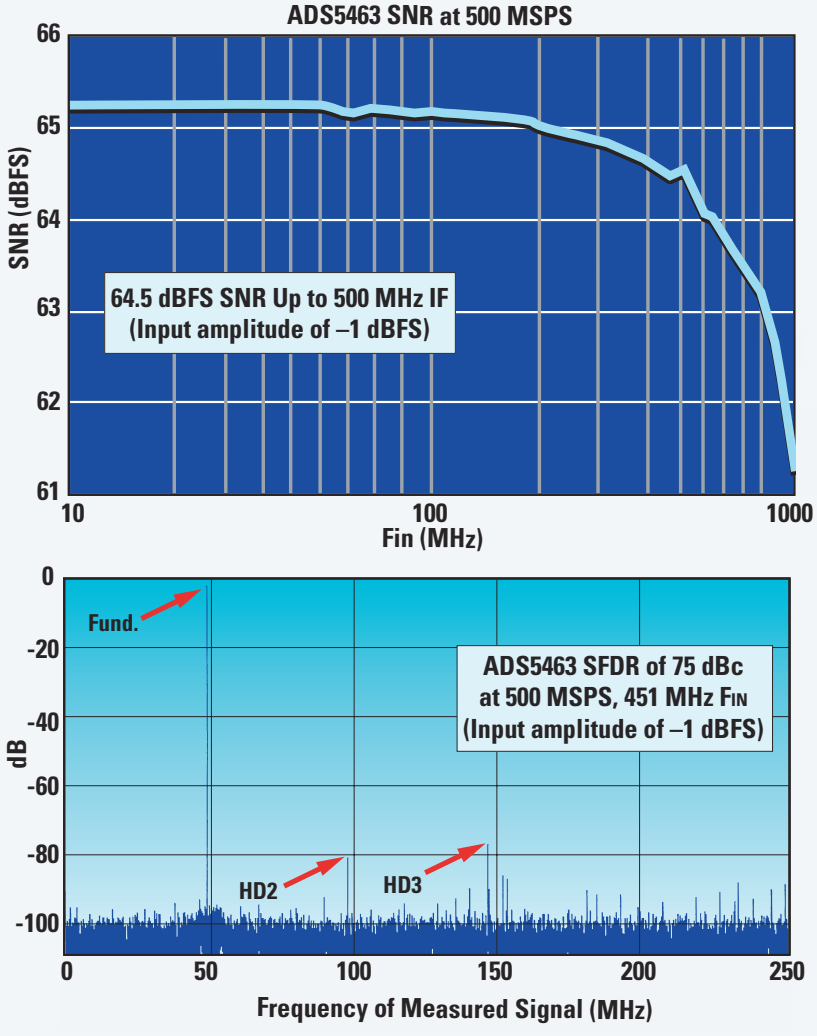
User-friendly model simplifies Spice op-amp simulation

DESIGNIDEAS



DATA CONVERTERS

12-Bit, 500 MSPS ADC



▶ Applications

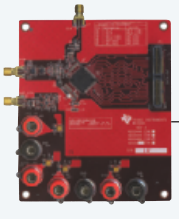
- Power amplifier linearization
- Multi-carrier receivers
- Software defined radio
- Radar and advanced imaging
- Test and measurement

▶ Features

- 12-bit resolution, 10.5 ENOB
- 2 GHz input bandwidth
- Space saving package size: 80-pin TQFP (14mm x 14mm)
- Differential input: 2.2 V_{PP}
- LVDS outputs with simplified data capture
- Total power dissipation: 2.25W
- Ind. temp: ADS5463 –40° C to +85° C
- Mil. temp: ADS5463-EP, QMLV –55° C to +125° C
- Pin-compatible with 13-bit, 210 MSPS ADS5440 and 13-bit, 250 MSPS ADS5444
- Recommended amplifiers: THS9000, THS9001, THS4304, THS4509, THS4511
- In production now: Priced at $125 in 1k units (Industrial temp. only)

The 12-bit, 500 MSPS **ADS5463** from Texas Instruments delivers best-in-class performance with greater than 75 dBc SFDR and 64.5 dBFS SNR for input frequencies through 450MHz. This new ADC benefits the most demanding amplifier linearization, communications, radar, imaging, test and measurement applications – all in a 14mm x 14mm 80-pin TQFP package. The ADS5463 is part of a pin-compatible family of products that include TI's 13-bit 250/210MSPS ADS5444 and ADS5440 ADCs.

For Evaluation Modules, Samples and Technical Information



www.ti.com/ads5463 ○ 800.477.8924, ext. 13476

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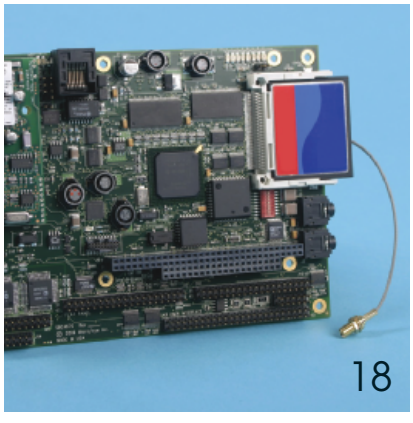

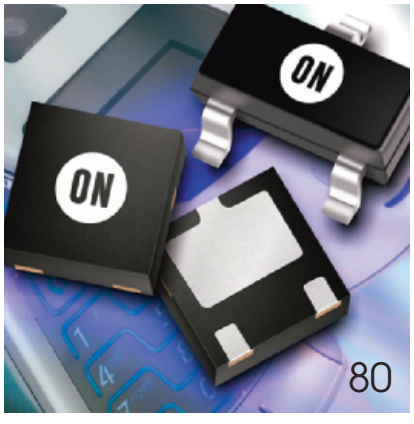

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Benefits of adding an active clamp to a synchronous flyback power supply
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Risk reduction in a verification upgrade
Chip-design managers cannot afford to wait for conclusive evidence before looking at adopting new verification methodologies. Therefore, it is important to have in place a good policy for minimizing the risks associated with adoption and assessing the impact of each change.
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Practical book helps developers apply USB-interfaced mass-storage devices
In technical writing, clarity is the name of the game.
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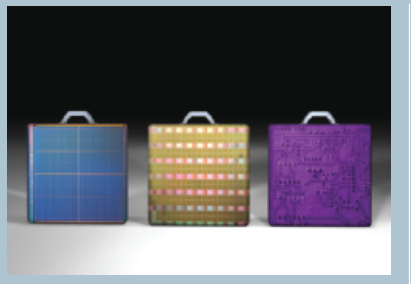

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BY MAURY WRIGHT, EDITOR IN CHIEF

Foggy crystal ball yields 2007 wishes

Well, 2007 has arrived, along with the New Year's resolutions and the ever-present pundit technology predictions. Unfortunately, my crystal ball is a bit foggy when it comes to such things as wireless LANs, video over Internet Protocol, UWB (ultrawideband), and home-video networks. So, rather than offer a set of predictions for tech in 2007, I'll offer a short list of wishes. Given the track record of the principals, I'm not confident that I'll see my wishes fulfilled. But I'm sure the tech industry would be better off if they do come true.

For starters, I'm hoping the IEEE 802.11n players finally come to an understanding. Their bickering hasn't stopped consumers from buying up Wi-Fi gear. Wi-Fi is now a standard feature in notebooks and is coming soon to handsets. But we've yet to have a chance to really figure out whether 802.11n might serve up whole-house video. I'm also just tired of the posturing and words such as "draft-n-compliant." And although I've been an Airgo supporter, the company even further crossed the line by declaring "draft-2.0" compliance with its recent chip announcement that coincided with the announcement that Qualcomm would acquire Airgo.

I'm also wishing for the streets in my neighborhood to be excavated once again. I hate the inconvenience but recognize that fiber must reach North American homes. AT&T has boasted that its U-Verse service is 100% video over IP. But AT&T isn't pushing fiber all the way to the home, and, even with VDSL2, the service provider will struggle to offer compelling HDTV services. Verizon is pushing fiber to homes, but mainly only in new developments or in areas where the company can string the fiber overhead. Meanwhile, Korea, Japan, and China are all working on massive fiber deployments. We need fiber for symmetrical data services and the best in video services, including true on-demand service. The last mile is still gating what can happen behind it in the core networks and in front of it in homes.

I hope the UWB crowd either finally delivers products in 2007 or just disappears.

I hope the UWB crowd either finally delivers products in 2007 or just disappears. The Wireless USB supporters that base the cable-replacement technology on UWB appear close. But most of the chip vendors had pledged that end products would ship for the 2006 holiday season. No luck there. I'm also unsure about how fast consumers will adopt a nice-to-have technology such as Wireless USB. The success may depend on how well it handles video, even over short distances. And Tzero Technologies is still claiming that its flavor of UWB can serve up whole-house video. If it does, I'll be first in line.

Perhaps my most fervent hope is that some industry players will again move toward the goal of building great products rather than chasing royalty streams. Sony has long been my favorite target in this regard. I was once one of Sony's biggest fans. At one time, my living room was all-Sony. Today a single, and admittedly dated, Sony DVD player is still present. Of late, Sony proves time and again that it cares more about getting IP adopted into standards such as next-generation DVD players than it does about building great products that consumers want to buy. The company isn't happy with just making money selling consumer products; it wants a slice of competitors' revenue as well, such as it has seen from the audio CD. It's increasingly clear that the strategy hasn't served Sony well; the company has lost status as a premium brand.

Unfortunately, the patent-troll philosophy isn't limited to Sony. Qualcomm has been guilty to some extent. Patriot Scientific comes to mind in the microprocessor area. It appears that former Microsoft executive and industry luminary Nathan Myhrvold plans to build a business around all types of IP with his Intellectual Ventures.

I'm not sure that we wouldn't be much better off with more open cross-licensing. One of the best interviews I did in 2006 was with Wally Rhines, Mentor's chief executive officer, in preparation for our 50th-anniversary issue last September. Rhines believes that massive cross-licensing in the early days of the semiconductor industry made for the explosive growth that we witnessed over several decades. We aren't seeing that growth these days. EDN

Contact me at mgwright@edn.com.

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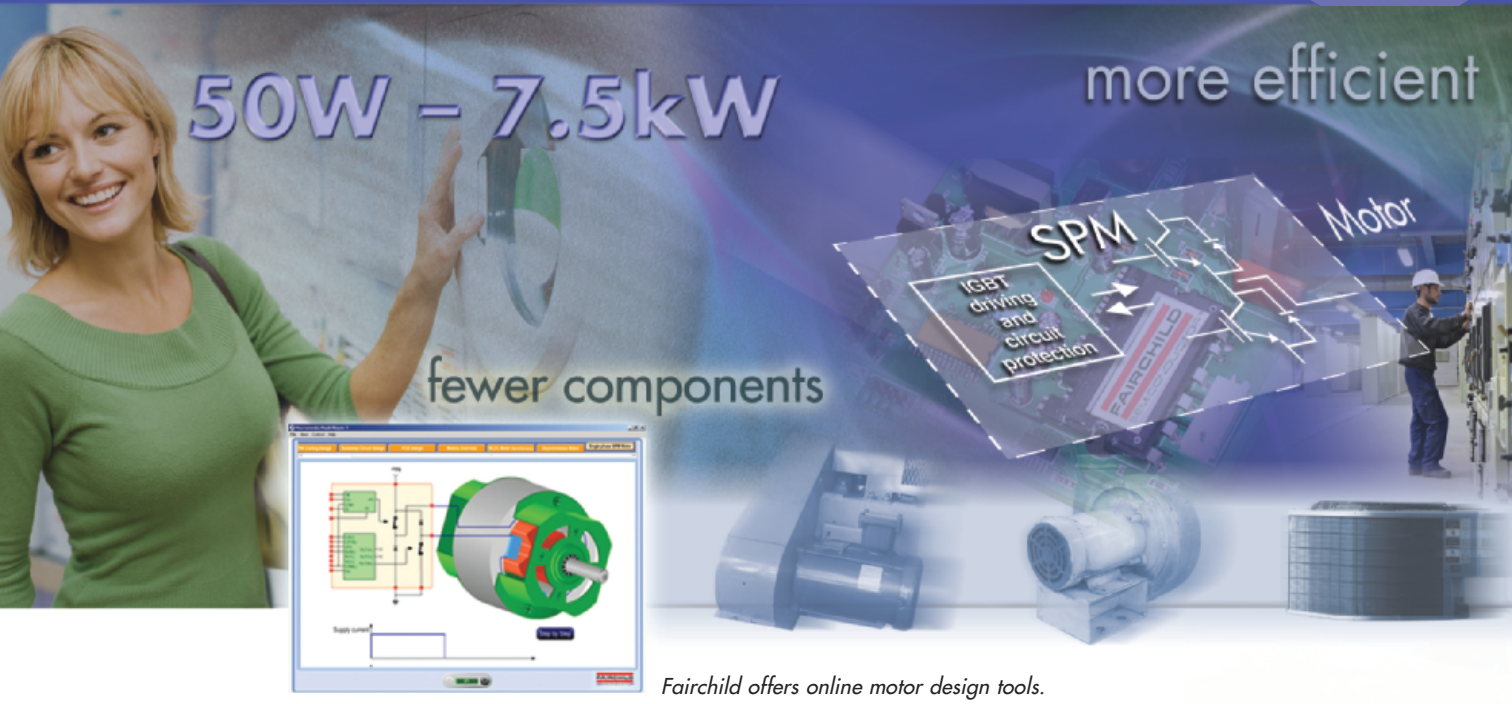

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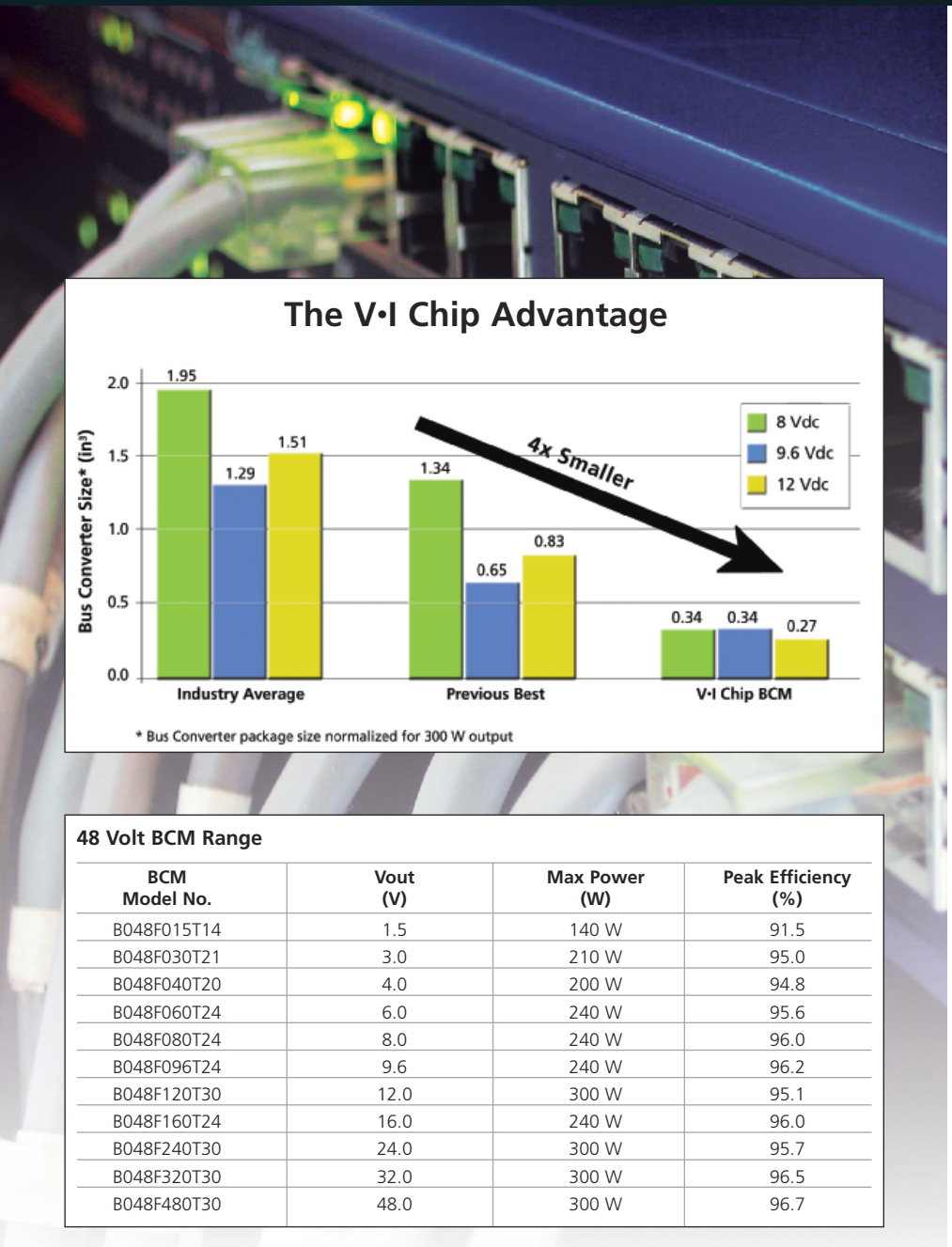

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48 Volt BCM Range

BCM Model No.	Vout (V)	Max Power (W)	Peak Efficiency (%)
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B048F030T21	3.0	210 W	95.0
B048F040T20	4.0	200 W	94.8
B048F060T24	6.0	240 W	95.6
B048F080T24	8.0	240 W	96.0
B048F096T24	9.6	240 W	96.2
B048F120T30	12.0	300 W	95.1
B048F160T24	16.0	240 W	96.0
B048F240T30	24.0	300 W	95.7
B048F320T30	32.0	300 W	96.5
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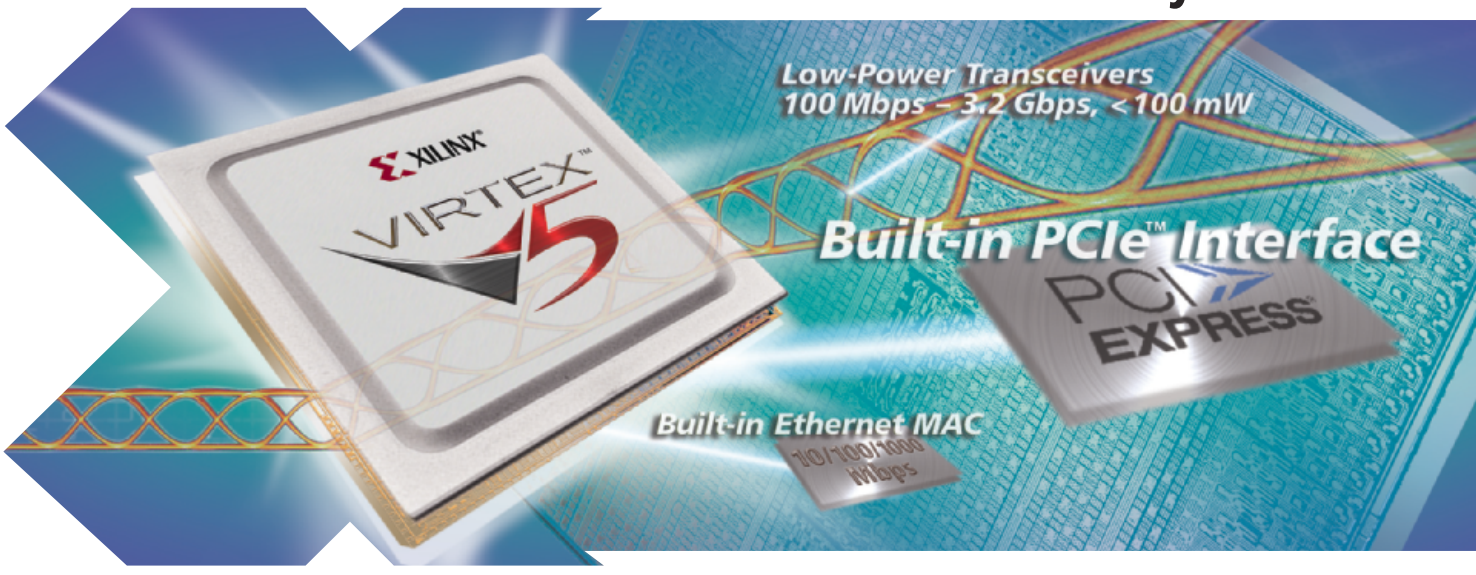

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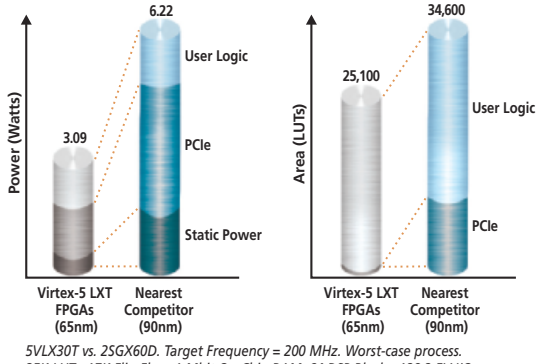

5VLX30T vs. 2SGX60D. Target Frequency = 200 MHz. Worst-case process. 25K LUTs, 17K Flip-Flops,1 Mbit On-Chip RAM, 64 DSP Blocks, 128 2.5V I/Os. Based on Xilinx tool v8.2 and competitor tool v6.0.1

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INNOVATIONS & INNOVATORS

High-speed modular logic analyzers capture as many as 512M samples

Agilent Technologies has expanded its logic-analyzer line with a new modular mainframe; two new modules, including one that provides four times the memory of the deepest memory logic-analyzer modules available from any manufacturer; and new applications for developers who use the PCIe (PCI Express) high-speed serial bus and Altera (www.altera.com) FPGAs.

Design teams in the computer, communications, semiconductor, aerospace, defense, automotive, and wireless industries continue to produce ever more complex high-speed-hardware designs. Validation and debugging of these designs necessitate increasingly capable logic-analysis tools. The 16900 product family addresses these requirements.

The two-slot, modular 16901A mainframe, with prices starting at $14,000, comes with a 15-in. display and a touchscreen interface that works well in applications in which limited bench space hinders the use of a mouse and keyboard. The mainframe allows connection and cross-triggering of other 16900-series mainframes in applications that require more than one logic analyzer.

The two-slot, modular 16901A logic analyzer sports a 15-in. touchscreen display.

The 68-channel 16950B logic-analyzer module, with prices starting at $23,500, offers state-analysis capture to 667 MHz at a maximum data rate of 1066 Mbps with as much as 64M samples of acquisition memory. The module offers the performance necessary to validate such leading-edge interfaces as DDR3 (double-data-rate 3) and front-side-bus designs.

The $65,000, 68-channel 16951B logic-analyzer module offers the same acquisition capabilities as the 16950B but quadruples the maximum memory depth to 256M samples, improving the probability that captured data will contain the flaw that caused a failure. Moreover, if you use only half of the channels, the memory depth doubles again—to 512M samples.

Two new applications speed the development of PCIe and Altera FPGA-based designs: The FSI-60112 PCIe Gen 1 probe, with prices starting at $24,700, supports the PCIe standard in one-, two-, and four-lane widths. When you use it with the 16800 portable logic analyzer, the probe offers what the manufacturer calls the market's lowest cost logic-analyzer-based PCIe-test approach. The B4656A FPGA dynamic probe, with prices starting at $3000, provides visibility into designs based on Altera FPGAs, thus speeding debugging and validation.

—by Dan Strassberg

▷**Agilent Technologies**, www.agilent.com/find/16900.

FEEDBACK LOOP

"Nothing beats wind power for common sense—so common that, while governor of Texas, George W Bush pushed for funding, support, and commitment to the effort that makes Texas the leader in wind power now. He ought to make the same moves from Washington now."

—Dick Davies in *EDN*'s Feedback Loop at www.edn.com/article/CA6399098. Add your comments.

PROCESSOR LOWERS COST OF GIGABIT ETHERNET

Freescale's MPC8313E PowerQuicc II Pro processor delivers Gigabit Ethernet with integrated security-encryption blocks for as low as $15 (10,000). It includes a dual 10-, 100-, 1000-Gbps Ethernet MAC (multiply/accumulate) unit with dual MII (media-independent interface), RGMII (reduced-Gigabit-MII), RTBI (reduced 10-bit interface), RMII (reduced MII), and SGMII (serial-Gigabit MII), and it supports the IEEE 1588 timing protocol. The Power Architecture e300 core operates at clock rates as high as 400 MHz. The device includes an MMU (memory-management unit); a USB 2.0 controller with an on-chip, 480-Mbps PHY (physical layer) with host and client support; a 32-bit PCI controller; and a 32-bit, 333-MHz DDR1/DDR2 (double-data-rate 1 and 2) memory controller. The integrated security engine provides hardware acceleration for the DES (Data Encryption Standard), 3DES (Triple DES), AES (Advanced Encryption Standard), SHA (Secure Hash Algorithm)-1, and MD (Message Digest)-5 algorithms.

The MPC8313E evaluation board sells for $299. It includes a Linux 2.6 BSP (board-support package) with the CodeWarrior-based development tools that include a six-month evaluation license with no code-size restrictions. The Linux 2.6 BSP includes drivers for SATA, a four-port GigESwitch from Vitesse (www.vitesse.com), USB, IEEE 1588, and power management. The evaluation-board reference design uses the MPC8313E, which includes a CPE (customer-premises-equipment) form-factor board, schematic, and layout.

Initial samples of the MPC8313E are available now, general samples should debut in the first quarter of 2007, and general availability is scheduled for the second quarter. The 516-pin PBGA device uses Freescale's 90-nm-process technology, and it supports 1V core operation and 1.8, 2.5, 3.3V I/O operation.

—by Robert Cravotta

▶**Freescale**, www.freescale.com.

Micro/sys' latest ARM-based single-board computer delivers Power-over-Ethernet technology plus multiple onboard communication interfaces.

EPIC computer expands communications options

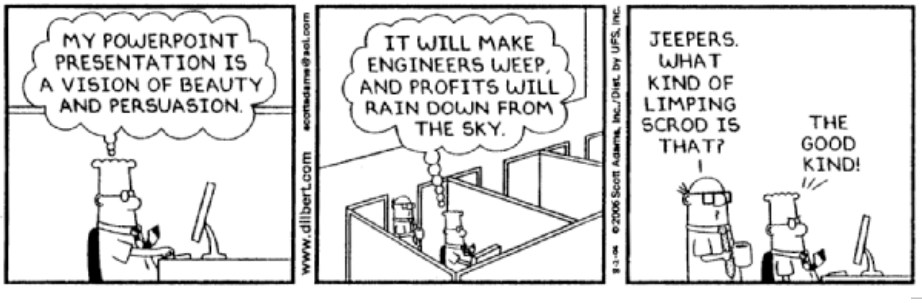
Targeting remote-terminal, data-logging, and protocol-conversion applications, Micro/sys recently introduced the SBC4670 single-board computer, which combines a low-power PX270 ARM (www.arm.com) processor with standard peripherals and multiple onboard communication formats. The SBC4670 provides optional support for serial protocols, including a socket modem for GSM/GPRS (Global System for Mobile communications/General Packet Radio Service) or Bluetooth wireless, a serial-CAN (controller-area-network) bus, GPS (global positioning system), five serial ports, and 10/100BaseT Ethernet. For control and monitoring applications, the board features eight channels of 14-bit ADC, eight channels of 14-bit DAC, and 24 channels of digital I/O. Available in a standard 4.5×6.5-in. EPIC (embedded-platform-for-industrial-computing) footprint, the SBC4670 also includes a watchdog timer, an SDRAM controller, a CompactFlash interface, and a USB-host controller. The board's 720-mA maximum-power draw allows you to power it remotely using POE (Power-over-Ethernet) technology.

The SBC4670 design includes a 16-bit PC/104 bus interface for access to many off-the-shelf boards, such as modems, analog I/O, or digital I/O. With 128 Mbytes of SDRAM and a 64-Mbyte resident flash array, the board supports the Linux, Windows CE, and VxWorks operating systems. Prices for the basic SBC4670 start at $595 (one), and an industrial-temperature (−40 to +85°C) version is also available for prices starting at $650. Prices for development kits begin at $950.

—by Warren Webb

▷**Micro/sys Inc**, www.embeddedsys.com.

DILBERT By Scott Adams



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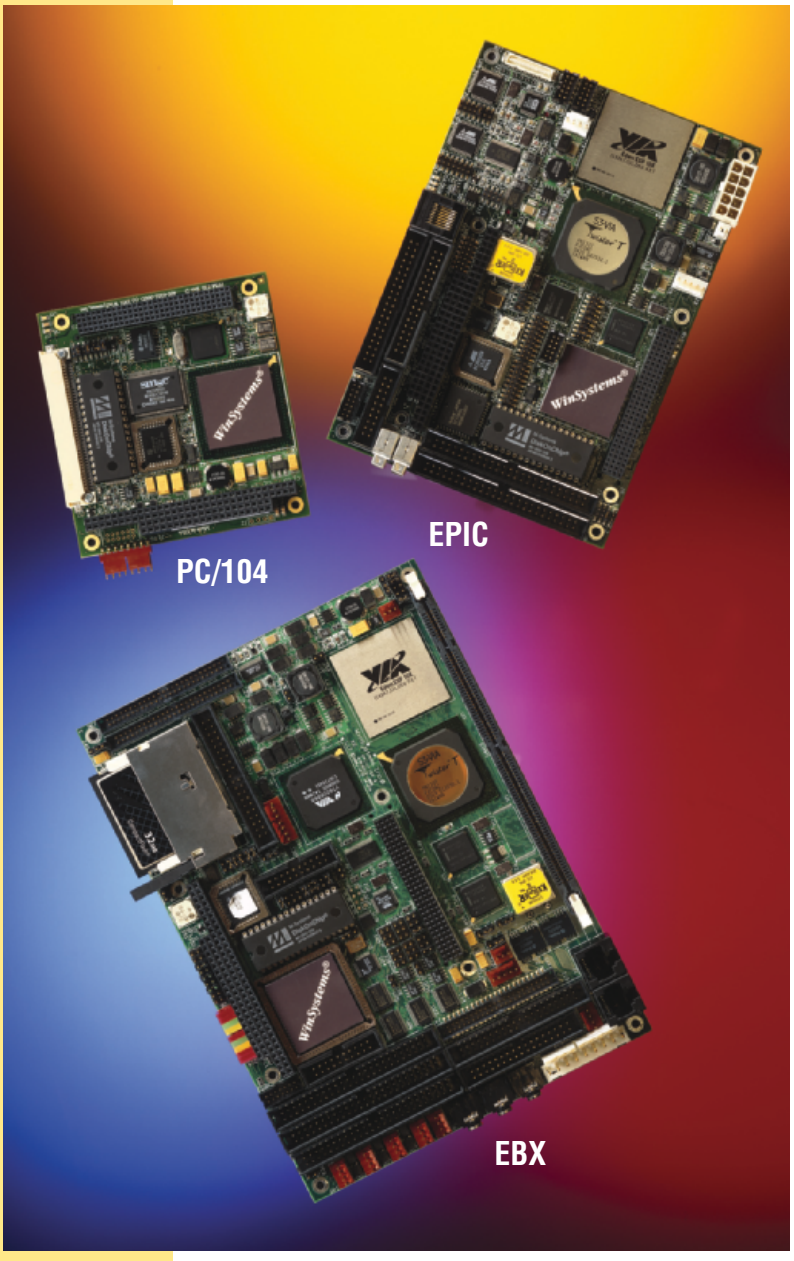

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ESL market adds an enterprise player

Cadence Design Systems Inc is making an enterprise-level play in the ESL (electronic-system-level)-software market by adding features to its Enterprise Manager environment, its Incisive Enterprise Simulator, and its new Palladium III emulator. Steve Glaser, corporate vice president of marketing in Cadence's verification division, says that most ESL-verification-tool flows now focus on the handoff between systems engineers (chip architects) and embedded-software developers. Glaser says, however, that ESL impacts several other disciplines in the flow and vice versa. These disciplines include hardware-design engineering, verification engineering, system-validation engineering and project management. Each of these disciplines interacts at some level, and the amount of interaction varies, depending on the nature of the design.

Glaser notes that the EDA industry hasn't yet produced a viable ESL-verification flow or even a tool to manage the scope of ESL within an enterprise. "The end goal of the customer is to get a predictable path to system quality and avoid re-spins. Even more important, errors at the system level can escape all the way to the end customer, … and product recalls can be enormously expensive," he says. "We're helping groups take a closer look at the complexities of their designs and giving them a way to manage the risks of those complexities—from spec and planning all the way to closure."

To accomplish this task, Cadence has extended its Incisive Enterprise Manager environment to form an ESL-flow-management system. Cadence last year released the Incisive Enterprise Manager. That product was a derivative of the vPlan and vManager products, which Verisity developed, and which Cadence acquired when it acquired Verisity in 2003. That version of Incisive Enterprise Manager allowed users to create an RTL (register-transfer-level)-to-gate-level verification plan to help design teams track verification progress and give them a better idea of whether they had done enough verification on a design. That version introduced management of assertion-based acceleration in PSL (Process Specification Language) and SVA (System Verilog Assertion) and transaction-based acceleration in SystemC and the e Testbench language. The version ran on the Incisive Enterprise Simulator and the Palladium II emulation system.

With this release, Cadence has extended the hardware-verification-plan and coverage-metric features of Incisive Enterprise Manager to embedded systems and software tools. Doing so allows enterprises to create ESL flows and track and analyze systemwide-verification activities, with the goal of refining the flow so that users can reduce time to market.

With this release, the company has also created an ESL option for its Incisive Enterprise Simulator. With the option, the simulator can now perform constrained random-scenario generation, and it includes a generic-software adapter that allows users to integrate embedded tools of their choice into the Cadence flow. The tool also supports the use of UVC (Universal Verification Component) verification IP (intellectual property). The UVCs send Incisive Enterprise Manager software subroutines in various sequences and measure coverage of those function calls. With the new ESL functions, users can also perform hardware-to-software debugging and failure analysis to test failures across the hardware-to-software boundary.

> "We're giving them a way to manage the risks of those complexities—from spec and planning all the way to closure.

The company has also added algorithms to Incisive Enterprise Manager and the ESL option to the Incisive Enterprise Simulator to allow the new Palladium III emulator to run in the ESL environment. Ran Avinun, product-marketing-group director in the system-level-verification group, says the new Palladium III includes a 256 million-gate top capacity and double the runtime and debugging performance of the Palladium II system. Emulation systems give users 100% visibility into the functions of their chip but typically run at speeds of only approximately 1 MHz. Furthermore, emulators are expensive. Avinun says that Palladium III will be attractive to traditional emulation users but that the new ties to ESL will potentially expand the usefulness of the emulation system to a broader number of users within an enterprise—groups looking at both hardware and software debugging.

Palladium III supports constrained random verification, as well as assertion-based acceleration in PSL and SVA and transaction-based acceleration in SystemC and the e Testbench language. Glaser claims that using Cadence's Enterprise ESL system will allow enterprises to cut time to market of IC projects by 50%. Prices for Enterprise Manager start at $70,000 for subscription licenses, and prices for the Enterprise Simulator start at $38,000. The ESL option costs $11,000 for users who own the simulator. Cadence sells Palladium III systems, but for users lacking million-dollar budgets, the company offers leasing and remote access to the system for prices starting at $150,000.

—by Michael Santarini

▷**Cadence Design Systems**, www.cadence.com.

FEEDBACK LOOP

"It is useful to turn the question 'what to do about energy supply?' on its head and ask 'what not to do?' And the answer to this question is clearly: 'Don't continue to grow populations.'"

—Tom Gosling in *EDN*'s Feedback Loop at www.edn.com/article/CA6399098. Add your comments.

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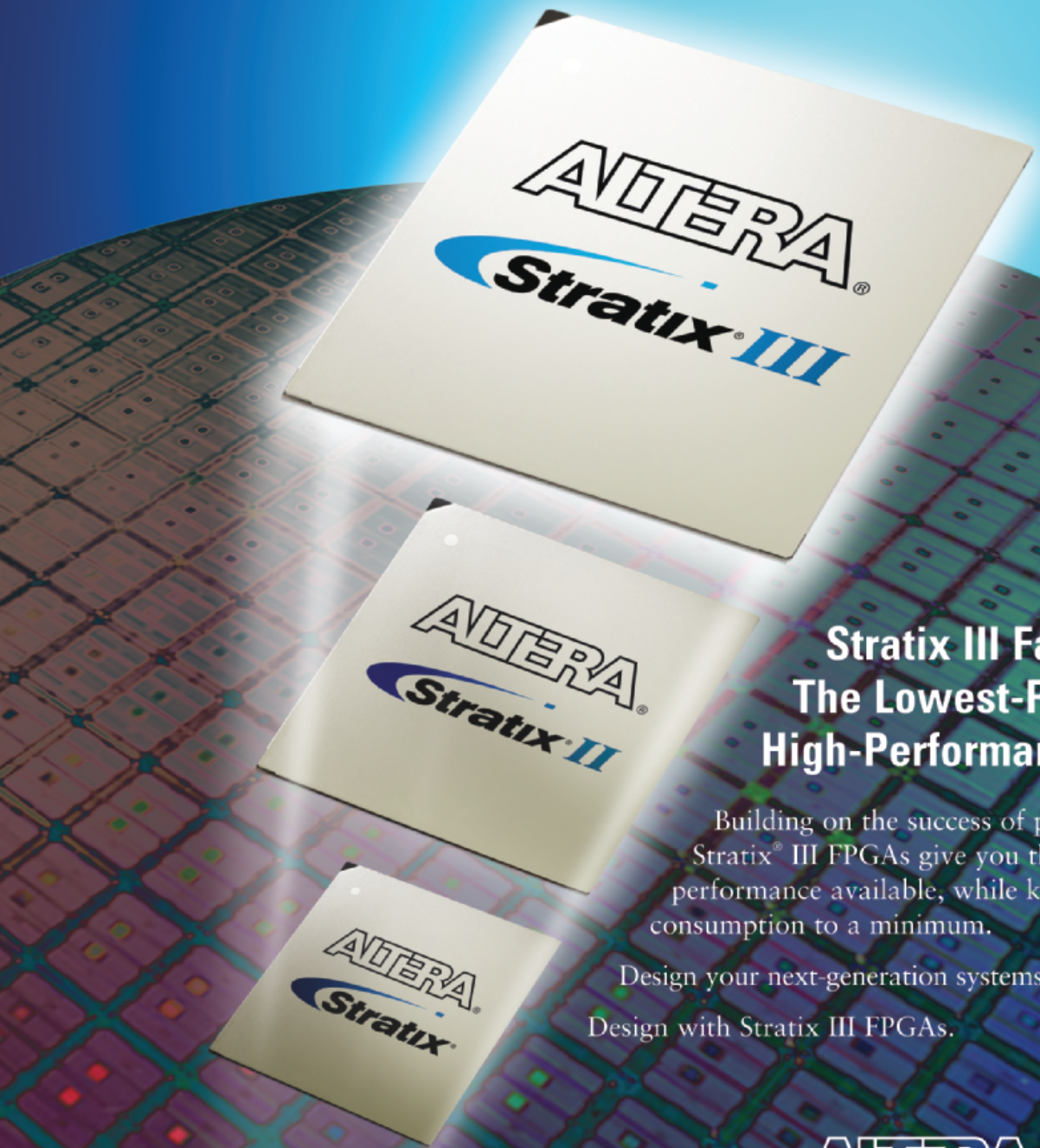

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Dummy-fill-synthesis tool has smarts

Blaze DFM is following up its mid-2006 release of its Blaze MO gate-CD biasing/leakage-control tool with an intelligent dummy-fill-"synthesis" tool. The tool addresses the problems that IC foundries encounter when they apply CMP (chemical mechanical polishing). Foundries apply CMP to each metal, via, and active polysilicon layer of a wafer to remove irregularities on the surface of each IC layer and to ensure that the layers have a smooth surface. But, in finer process geometries, CMP often errantly creates its own topographical variations—nonuniform layers, or "dishing"—causing the features to work improperly. The CMP process can sometimes scrape away too much metal or distort features, causing electromigration or shorts. All these CMP-related problems adversely affect yield and product reliability. To counter CMP-dishing effects, engineers usually add dummy fill to even out layers.

Dave Reed, Blaze DFM's vice president of marketing, says that engineers have traditionally relied on DRC (design-rule-correction) scripts to determine the best places to insert dummy fill. Reed notes that, with every new process, the number of rules for CMP grows exponentially and the rules are typically too generalized, applying the same amount of fill if it fits a general situation. "Rules-based [fill] is what everybody has been using, but model-based is where everything is heading," says Reed. "We've been working closely with the foundries on their CMP models. The models are much easier to maintain and enhance than these rules-based scripts, and we're not even sure if people will be able to go even one more generation with these DRC scripts. Even today, they can't get an optimal result with just CMP scripts."

Working at 65-nm processes, companies are also now adding polysilicon fill to polysilicon layers to make the shapes look more regular for lithography tools, further complicating scripting. Andrew Kahng, PhD, the company's co-founder and chairman, and his team at the University of California—San Diego have found a way to formulate the fill problem so that solvers can solve it.

The Blaze IF tool reads CMP models from foundries and scripts from DRC tools. Third-party timing- and power-analysis tools provide data to the tool, and it inserts dummy fill into design layouts to ensure density uniformity and thickness. "We think it will be used at the end of place and route," says Reed. "Anybody who knows timing, which will be the physical-design folks, should take responsibility for this now. Previously, this step took place during DRC. We don't think the physical-design guys should be responsible for your timing."

Users feed the tool SPEF (standard-parasitic-exchange-format), SDC (Synopsys-design-constraint), Verilog, and VCD (Verilog-change-dump) files, along with a post-place-and-route database of LEF (library-exchange-format), DEF (data-exchange-format), GDSII (Graphic Design System II), and OA (Open Access) database files.

Cypress Semiconductor (www.cypress.com) was one of the tool's beta testers. On a project in 90-nm silicon, Cypress maintained ILD (interlayer-dielectric)-thickness variation that was 56% less than the company achieved with its own advanced-fill method. Reed says that figure is especially impressive given that Cypress' fill method afforded the company only a 2% ILD improvement over using no fill at all. Blaze DFM licenses the Blaze IF for a $250,000 annual subscription.

—by Michael Santarini

▷**Blaze DFM Inc**, www.blaze-dfm.com.

01.04.07

WIQUEST ADDS VIDEO SUPPORT TO WIRELESS USB

For months now, rarely a week has passed when one Wireless USB player or another hasn't touted a chip compatible with the specifications that the WiMedia Alliance (www.wimedia.com) has shepherded. Based on UWB (ultrawideband) technology, broadly shipping Wireless USB products should hit the shelves in the first quarter of this year. After what seems like years waiting for the technology, you should expect a number of product announcements at the CES (Consumer Electronics Show, www.cesweb.org), which will take place Jan 8 to 11 in Las Vegas. Most of the recent buzz has been posturing about compliance with WiMedia standards. WiQuest, however, appears to be moving ahead with real products. The company has been on the forefront of FCC certification with its silicon. It recently received the alliance's certification for a Wireless USB-hub reference design. Although the end-product maker must ultimately earn certification, having the chip company go through the process with a reference design greatly eases the burden on the end-product manufacturer. Moreover, in mid-December, the company announced a video-enabled addition to its chip family.

The new chip set, WiDV (wireless digital video), enables in-room distribution of video, along with general Wireless USB capabilities. WiQuest's ICs support 1-Gbps data rates, which exceed the 480-Mbps rates that the Wireless USB standard specifies. Further, the company has added a proprietary video-compression capability to the latest WQUST100 chip set. Those features combine to enable transmission of HDTV-quality video over a range of 2 to 3m. The company foresees both PC and living-room applications for the new chip. For more on the chip set and a list of other players in the market, go to www.edn.com/article/CA6401216.—by Maury Wright

▶**WiQuest, www.wiquest.com.**

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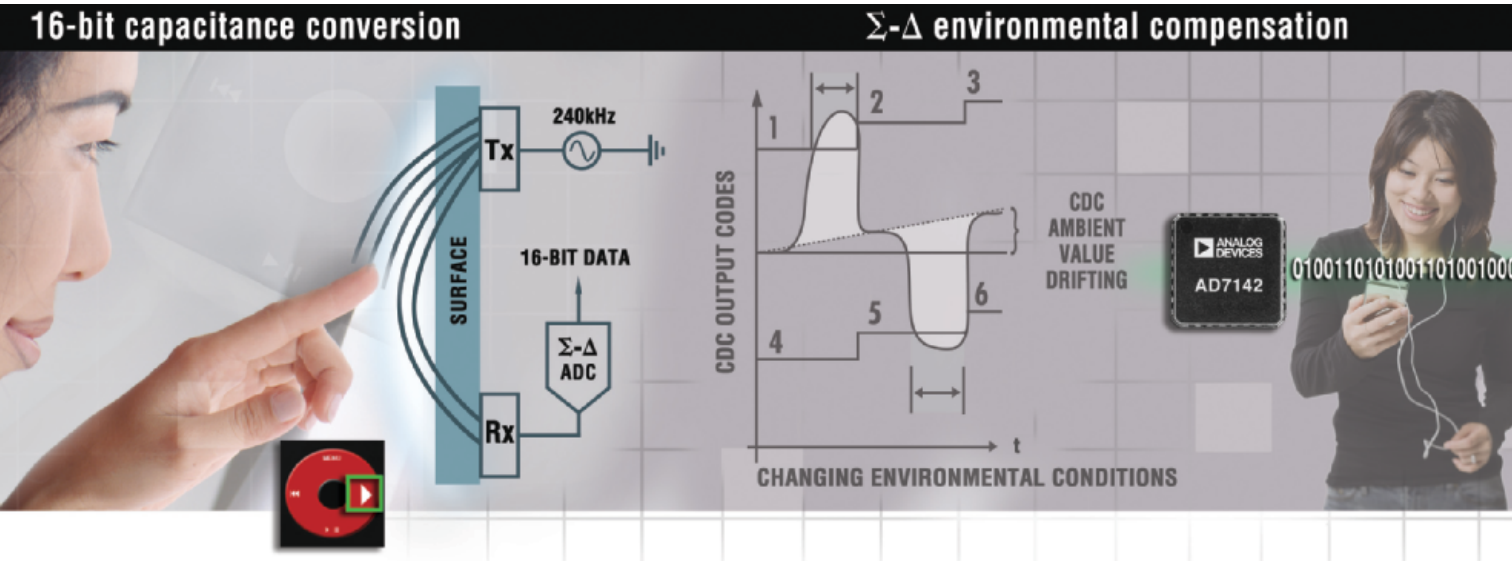

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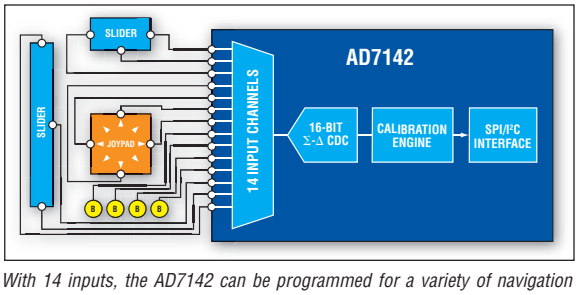

With 14 inputs, the AD7142 can be programmed for a variety of navigation functions including buttons, sliders, scroll wheels, and joypads.

Improved sensitivity and environmental calibration—made possible by Σ-Δ conversion

For products with increasing feature convergence, finger-driven navigation enhances the user experience—for designers as well as consumers. The AD7142 capacitance-to-digital converter (CDC) with on-chip environmental compensation delivers unmatched touch control performance. It offers:

- Reliable performance over supply and temperature
- Programmable functionality and touch sensitivity
- 50% lower power than competitive solutions
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ADI also offers CDC solutions for measuring proximity, position, level, pressure, and humidity.

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ANALOG DEVICES

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Point-and-see picture transfer requires no setup, employs IrDA

As a long-term supplier of transceivers to the IrDA (Infrared Data Association) market, Sharp Microelectronics is promoting the IrSimple "special case" of that standard for sending pictures from camera phones to televisions. Sharp expects that this task—informal sharing of pictures among family or colleagues—will be an attractive feature for camera-phone makers to offer. IrSimple allows fast picture transfer with virtually no setup procedure. Compared with the original IrDA specification—possibly one of the most widely deployed yet least-used interfaces—IrSimple increases transfer speed by stripping off most of the preamble and postdata "wrapping" that IrDA uses to ensure correct transmission and to facilitate retransmission of data blocks if any data is missing or corrupted. According to Sharp, the rationale is that, in the case of sending a picture for immediate display, users have equally immediate feedback if the transmission has failed; they see a poor picture or no picture at all. In that case, they can retransmit the picture themselves without the overhead of a protocol to do it for them.

The raw data rate remains the same as with IrDA 1.3: 4 Mbps. With the "reduced" protocol, the connection-setup time is 0.2 seconds as opposed to 3 seconds, and almost all the 4-Mbps data rate is available to deliver the payload, as opposed to an effective rate of approximately 500 kbps with IrDA. The overall effect, Sharp says, is that a typical JPEG of 150 kbytes takes 0.5 seconds in IrSimple versus 5 seconds in IrDA. The company contends that the usage model—point the phone at the television from approximately 1m away and see the picture almost instantly—is an intuitive process that suits the task and may do the same for other informal, "closed-system" data transfers at lower cost than alternatives, such as Bluetooth or Wi-Fi. Bluetooth Version 1.1, Sharp points out, would take more than 30 seconds to transfer the same picture.

—by Graham Prophet, *EDN Europe*

▷**Sharp**, www.sharpsme.com.

POWERING SOCs WITH INTEGRATED APPROACHES

A typical portable electronic device, such as a mobile phone or an MP3 player, comprises a variety of chips—many of which need different power-supply voltages. For instance, USB OTG (on the go) needs a 5V source, analog sections and interfaces require 3.3V, and RF chips need 2.5 and 1.8V sources. To compound the issue, current requirements for the chips vary, as does the quality of the power. Design engineers usually resort to a plethora of power-supply regulators with varying voltage, current, and noise specifications to meet the power demand, which results in a proliferation of power-regulator chips, consumption of precious board space, and increased bill-of-material costs. Spotting an opportunity, Cosmic Circuits has created a set of IP (intellectual-property) cores that can integrate power regulators on an SOC (system on chip) to reduce component count and costs. The company has created about 10 types of power circuits in its Power-On SoC family on 130- and 90-nm TSMC (Taiwan Semiconductor Manufacturing Co, www.tsmc.com) process technology for various portable applications, including wireless LANs, MP3 players, UWB (ultrawideband) systems, and connectivity devices.

According to Krishnan Ramabadran, vice president of Cosmic Circuits, the principal challenge in designing the IP cores was to achieve high power efficiency in dc/dc-switching converters for battery-powered applications, even at low load currents. The space-constrained environment of portable electronic systems also means that Cosmic had to design the cores in a way that would minimize the size of the inductors and capacitors on the board. The team also had to tackle 5V in a deep-submicron process to avoid the need for a step-down converter.

The company is now claiming a few industry firsts with its IP cores: a buck-boost converter that operates as low as 2.7V to extract the last bit of juice out of a battery; low-dropout regulators with a PSRR (power-supply-rejection-ratio) as high as 50 dB at 1 MHz; greater-than-90%-efficient capacitive switching regulators or charge pumps for supplying power to LEDs; a lithium-ion-battery charger that integrates a charging transistor in 130-nm digital-CMOS technology; and a super-low-power, low-dropout regulator that supplies trickle power to real-time-clock circuitry.

With many of the power blocks offering features and performance levels previously unavailable as IP to fabless companies, Cosmic is hopeful that it can become a supplier of choice to semiconductor-design houses in the consumer-electronics market. Ramabadran concedes that some applications may not benefit from this kind of power-management integration. For example, systems that require load currents exceeding 2A or those operating at input voltages of 9 to 12V could work equally well with designs based on discrete components rather than an SOC-integrated approach.—by Chitra Giridhar, *EDN Asia*

▶**Cosmic Circuits, www.cosmiccircuits.com.**

01.04.07

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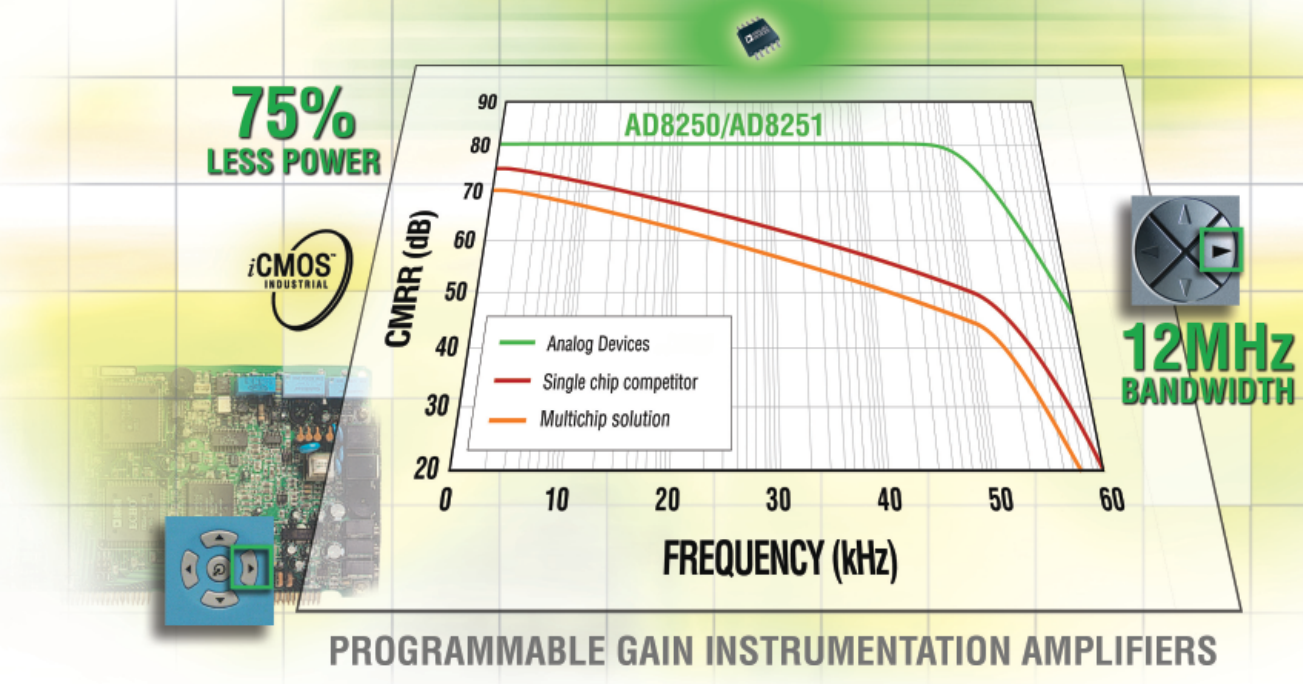

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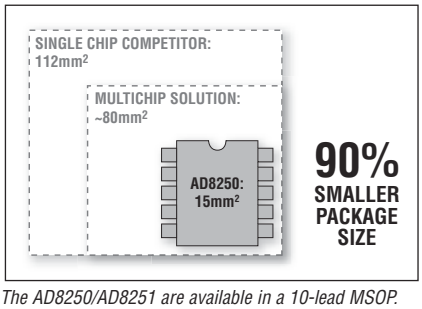

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ANALOG DEVICES

BY HOWARD JOHNSON, PhD

Two-way street

Suppose that I gave you a highway-traffic monitor that reports total traffic density on a section of roadway but does not provide separate figures for eastbound and westbound traffic. Obviously, this sensor reveals only part of the total traffic picture. Transmission lines, like streets, support traffic in two directions. A voltage probe connected to a transmission line acts much like a traffic-density sensor. It shows an aggregate-voltage waveform but doesn't say *which way the waveform is moving*.

For example, **Figure 1** shows the composite voltage (pink) at capacitor C_3 (**Reference 1**). The waveform shows a 200-psec step followed by a negative bump at B. To decipher the cause of that bump, include in your schematic a virtual (nonphysical) 0Ω resistor, R_0. Set all the parasitics associated with that component to their minimum values.

Transmission lines, like streets, support traffic in two directions.

Export from your simulator both the voltage, v_0, at R_0 and the current, i_0, flowing through R_0. Then, use the equations in **Figure 1** to compute both forward- and reverse-moving waveforms, v_F and v_R, respectively.

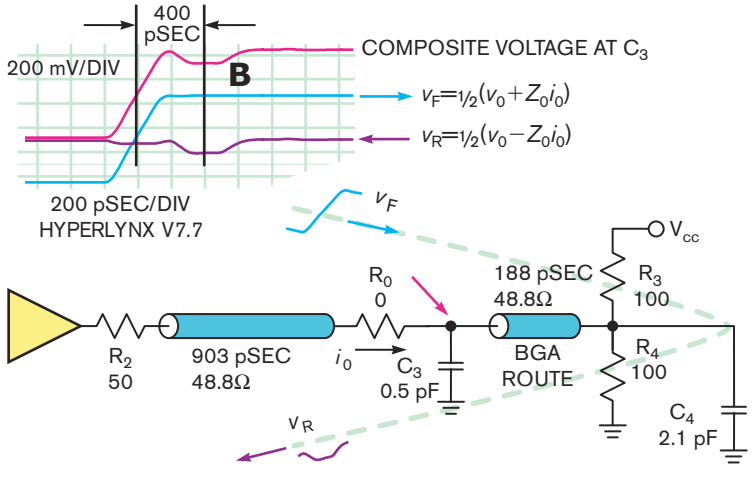

Figure 1 Voltage waveforms v_F and v_R propagate in opposite directions.

The composite waveform at C_3 is the sum of these two waveforms. The forward waveform (blue) appears ideal. The negative bump appears only in the reverse waveform (purple). Therefore, the bump must be a reflection coming from something to the right of C_3.

Next, consider the shape and timing of the reflected bump. The bump duration is comparable with the signal rise time, so you may conjecture that it comes from one localized spot. The center of the bump occurs 400 psec after the midpoint of the initial rising edge. That 400-psec number is a round-trip reflection delay, so the imperfection you seek must be 200 psec downstream from R_0. The only significant imperfection near that location is the receiver-load capacitance, C_4. If you remove C_4 from the circuit, the bump disappears, confirming C_4 as the source of the bump. A thorough examination of v_R reveals a second negative bump, smaller than the first, coincident with the main signal edge. That reflection comes from the C_3.

If this technique seems new or unusual to you, think back to when you were a little kid. Didn't your mother tell you to look both ways? EDN

REFERENCE

1 Johnson, Howard, PhD, "Eye of the probe," *EDN*, Dec 1, 2006, pg 30, www.edn.com/article/CA6395495.

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Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his Web site at www.sigcon.com or e-mail him at howie03@sigcon.com.


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BY BOB MASON • SCHNEIDER ELECTRIC/SQUARE D

Testing our reliance on testing

DANIEL VASCONCELLOS

In the late 1980s, my company was in the market for its first CAE (computer-aided-engineering) system. Because we did a lot of mixed-signal design, we were particularly interested in being able to simulate those kinds of circuits. We developed a series of benchmark tests that included pure-digital circuits, pure-analog circuits, and one mixed-signal circuit. We based all of these circuits on real-life designs that we had recently worked with.

We were particularly careful when choosing the mixed-signal circuit. We wanted to have a realistic test but one that would also challenge the simulator. The circuit we chose, a microprocessor-controlled 4- to 20-mA converter, was ideal. We had thoroughly wrung out the design, through both analysis and testing, so we knew exactly how it worked. The circuit was in production and working flawlessly. We could control the simulations to drive the simulator to any circuit condition we wanted. We could control data to check response times and compare transient responses between the simulation and the real world. My team was ready for anything!

The first companies to get our testbench couldn't even begin to simulate the mixed-signal circuit. The output never got close to 20 mA. We gave each other smug looks and muttered: "Another case of marketing hype."

The last company to get the circuit was having trouble, too. The company's field-applications engineer called us up one day to talk about his problems.

"You say this is a working design?" he asked.

"Yes," we replied. "It is in production and working perfectly."

"Well, my simulations can't get the circuit to drive up to 20 mA; it stops well below that." Again, my team members and I gave each other knowing looks. "But, when I changed the op-amp model from worst case to nominal, it started working." You could hear a pin drop in the room.

It turns out that the simulator's model assumed a worst-case supply-rail-to-output drop, resulting in less output swing than we needed. That worst-case drop prevented a pass transistor from fully turning on. Our vaunted circuit design was a dud! Despite exhaustive testing, we had never encountered an op amp with that much output drop. The analysis had missed it. It turns out that the designer felt that a worst-case analysis of the circuit was too difficult, so he ran "lots of tests." This situation was another example of why not to rely on testing to determine a design's limits: You will rarely encounter worst-case parts.

Epilogue: We quietly implemented an engineering-change notice to change resistor values in the circuit so that it would work at worst-case conditions. We also bought that company's simulator and showed the designer how to run worst-case and Monte Carlo analyses. EDN

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Bob Mason is a senior engineer in the Engineered Solutions Center at Schneider Electric/Square D. Like Bob, you can share your Tales from the Cube and receive $200. Contact Maury Wright at mgwright@edn.com.

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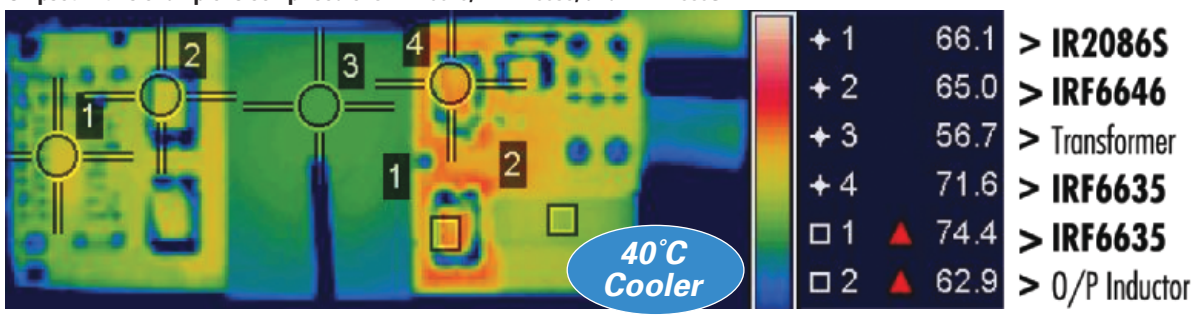

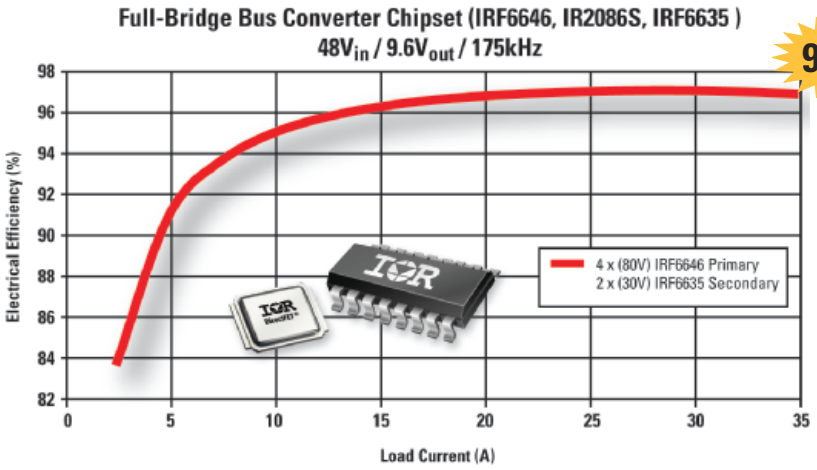

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IRF6655	Small can	100V	62mΩ	8.7nC	2.8nC
IRF6646	Medium can	80V	9.5mΩ	36nC	12nC
IRF6638	Medium can	30V	2.9mΩ	30nC	11nC
IRF6635	Medium can	30V	1.8mΩ	47nC	17nC
IRF6631	Small can	30V	7.8mΩ	12nC	4.4nC
IRF6629	Medium can	25V	2.1mΩ	34nC	11nC
IRF6628	Medium can	25V	2.5mΩ	31nC	12nC
IRF6622	Small can	25V	6.3mΩ	11nC	3.8nC

Control IC			
Part #	Package	Voltage Rating	Description
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Under the hood of hybrid vehicles

Energy- and emission-efficient automobiles are increasingly relying on both combustion engines and electric motors for power.

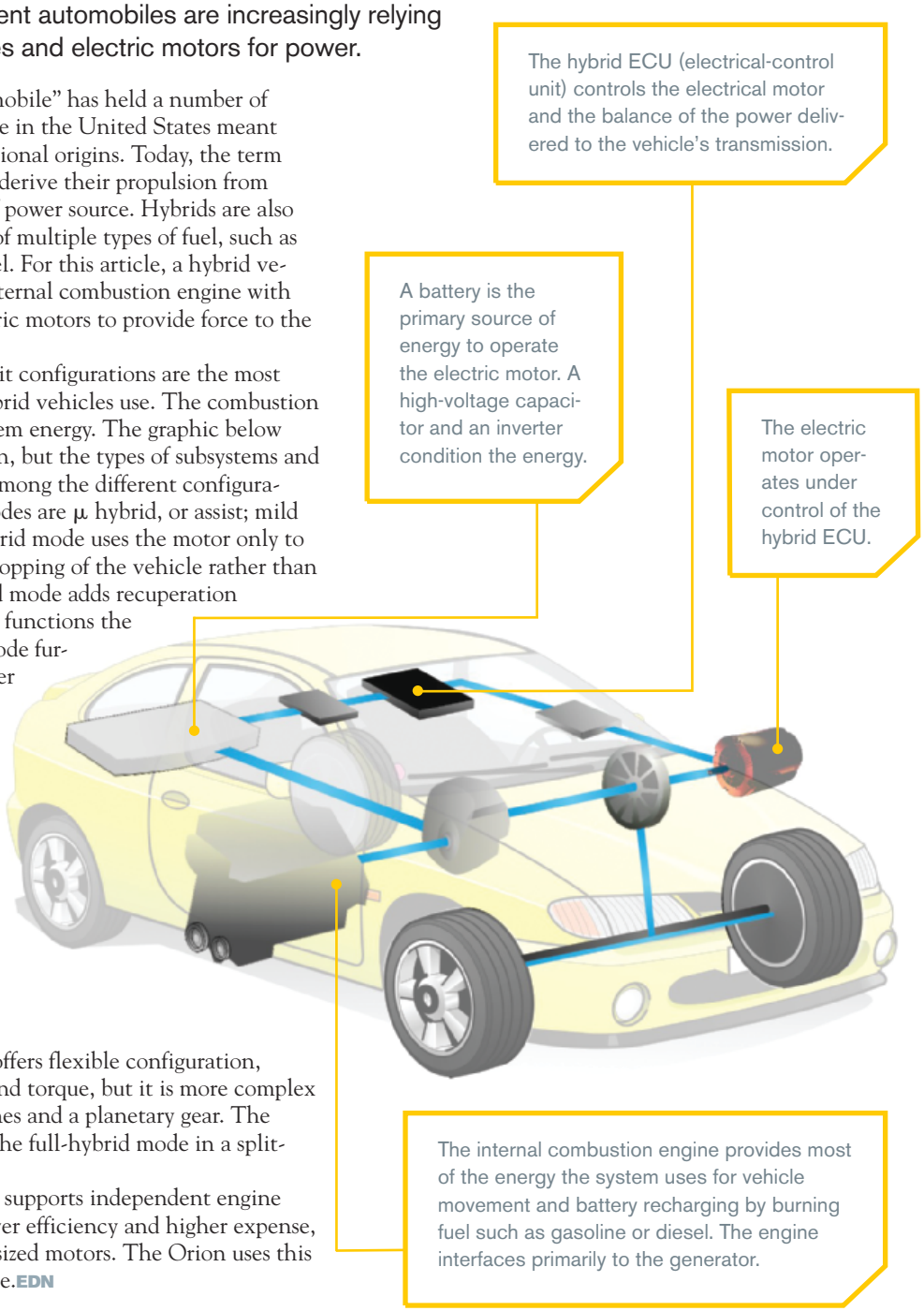
The term "hybrid automobile" has held a number of meanings. An early use in the United States meant a vehicle of mixed national origins. Today, the term refers to vehicles that derive their propulsion from more than one type of power source. Hybrids are also vehicles that can use a mixture of multiple types of fuel, such as gasoline and ethanol-alcohol fuel. For this article, a hybrid vehicle is one that combines an internal combustion engine with electric batteries powering electric motors to provide force to the vehicle's wheels.

Parallel, serial, and power-split configurations are the most common configurations that hybrid vehicles use. The combustion engine provides most of the system energy. The graphic below shows a power-split configuration, but the types of subsystems and components are mostly similar among the different configurations. Three common hybrid modes are μ hybrid, or assist; mild hybrid; and full hybrid. A μ-hybrid mode uses the motor only to support improved starting and stopping of the vehicle rather than for fuel efficiency. A mild-hybrid mode adds recuperation and acceleration boosting to the functions the motor supports. A full-hybrid mode further adds the ability for the power from the motor to supersede the combustion engine for electric driving.

A parallel configuration provides higher efficiency, easier integration, and lower additional cost to the engine system. However, it couples the engine and motor speed. The Citroen C3 and the Honda Civic have used a parallel configuration in μ-, mild-, and full-hybrid modes.

A split-power configuration offers flexible configuration, which optimizes drive comfort and torque, but it is more complex because it requires two e-machines and a planetary gear. The Toyota Prius and the Lexus use the full-hybrid mode in a split-power configuration.

A serial-hybrid configuration supports independent engine operation, but it suffers from lower efficiency and higher expense, because the system has two full-sized motors. The Orion uses this configuration in full-hybrid mode. EDN



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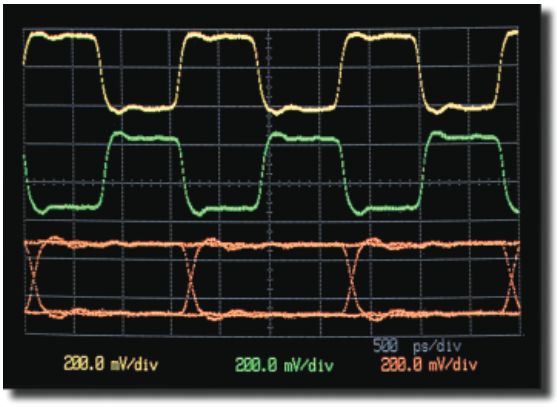
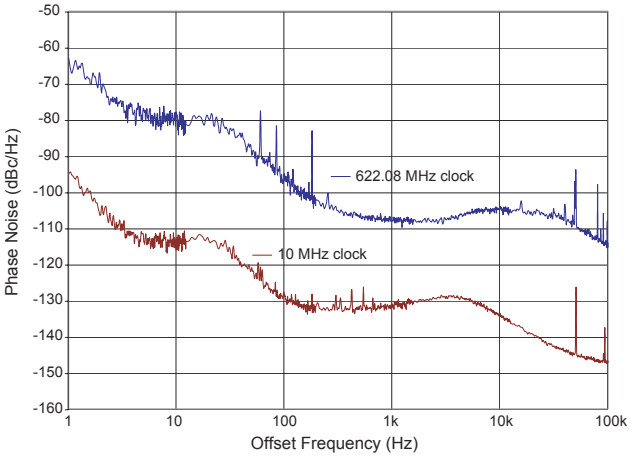
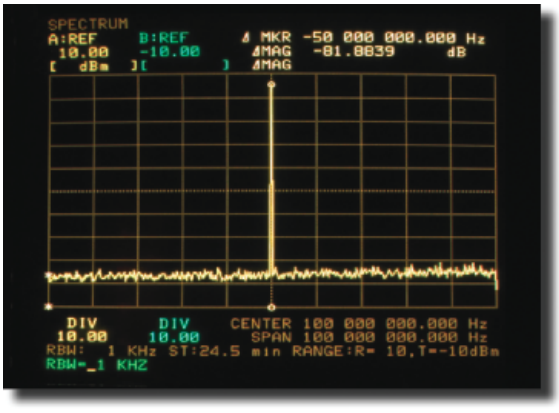


Clock and PRBS signals at 622.08 MHz

Plot shows complementary clock and PRBS (opt. 1) outputs at 622.08 Mb/s with LVDS levels. Traces have transition times of 80 ps and jitter less than 1 ps (rms).



Phase noise for 10 MHz and 622.08 MHz outputs



RF Spectrum of a 100 MHz clock

Graph shows a 100 MHz span around a 100 MHz clock. Only two features are present: the clock at 100 MHz, and the spectrum analyzer's noise floor (around –82 dBc).

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Clocking High-Speed A/D Converters

Application Note AN-1558

James Catt, Applications Engineer

Extremely high-speed ADCs (>1 GSPS) demand a low-jitter sample clock in order to preserve Signal-to-Noise Ratio (SNR). These 8- and 10-bit converters have best-case noise floors set by quantization noise. For an N-bit ADC sampling a full-scale sinusoid, the well known expression for SNR (in dB) is: SNR = 6.02N + 1.76. This sets the best case noise floor for an 8-bit ADC at -49.9 dBc. The noise floor degrades from this point due to factors such as jitter on the sample clock, intrinsic aperture jitter of the ADC, spurious components arising from non-linearities in the ADC quantizer, and other internal noise such as thermal noise. In this article, we look at the strategy for optimizing the performance of the sample clock based on PLL/VCO characteristics. This means minimizing overall integrated phase noise, which minimizes clock jitter.

The Root-Mean-Square (RMS) jitter of the sample clock combines with the intrinsic RMS aperture jitter of the ADC in a root-sum-square fashion to produce a total affective jitter. Total RMS jitter is:

$$\sigma_T = \sqrt{\sigma_{Clk}^2 + \sigma_{aperture}^2} \qquad \textit{Equation 1}$$

The SNR due to total jitter is:

$$SNR_{dB} = 20 \cdot \log\left(\frac{1}{2\pi f_{in}\sigma_T}\right) = 20 \cdot \log\left(\frac{1}{2\pi f_{in}\sqrt{\sigma_{Clk}^2 + \sigma_{aperture}^2}}\right) \qquad \textit{Equation 2}$$

Solving for the maximum allowable clock jitter given some target SNR and ADC aperture jitter:

$$\sigma_{Clk} \le \sqrt{\frac{1}{(2\pi f_{in})^2 \cdot 10^{\frac{SNR}{10}}} - \sigma_{aperture}^2} \qquad \textit{Equation 3}$$

The aperture jitter specification for National's ADC08D1500 8-bit, 1.5 GSPS converter is 400 femtoseconds (fs.). Using this value and a maximum input frequency of 748 MHz (f_{IN}), ***Table 1*** lists the allowable sample clock jitter for target SNR due to total jitter.

The third column of the table shows the combined SNR due to quantization noise and jitter for an 8-bit ADC, using a quantization noise SNR of 49.9 dB.

The allowable jitter (column 2) required to achieve a total SNR that is close to 49.9 dB is extremely difficult to achieve at a reasonable cost. However, achieving RMS clock jitter below 500 fs is possible using National's LMX2531LQ1500E frequency synthesizer combined with a high quality crystal reference oscillator. The LMX2531LQ1500E is shown in ***Figure 1.***

Target Jitter SNR (dB) (Aperture and Clock Jitter)	Allowable Clock Jitter (fs)	Total SNR Due to Quantization Noise and Jitter (dB) $SNR = 10\log\left(\frac{1}{\frac{1}{10^{\frac{SNR_J}{10}}} + \frac{1}{10^{\frac{SNR_Q}{10}}}}\right)$
54	142	48.5
53	259	48.2
52	354	47.8
51	447	47.4
50	541	46.9
49	640	46.4
48	747	45.8
47	862	45.2
46	989	44.5

Table 1. Jitter SNR and Allowable Clock Jitter, with Total SNR

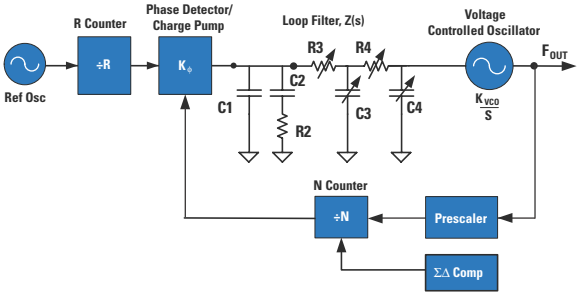

Figure 1. LMX2531LQ1500E Simplified Block Diagram

For this example, we use the LMX2531LQ1500E to generate a fixed 1.5 GHz sample clock that can drive any of National's GSPS ADCs. Because the ADC clock is fixed, we can design the loop filter to achieve optimized phase noise performance, giving best jitter performance. Each functional block in ***Figure 1*** contributes some form of noise. The following table lists the low and high

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frequency approximations for their noise transfer functions.

Noise Source	Low Frequency Transfer Function Approximation	High Frequency Transfer Function Approximation
Reference Oscillator	N/R	G(s)
R Divider	N	G(s)
N Divider	N	G(s)
Phase Detector	N/Kϕ	G(s)

Table 2. Noise Transfer Functions, T(f)

Source: Dean Banerjee, PLL Performance: Simulation and Design, 4th Edition, Dogear Publishing, Indianapolis, 2006.

G(s) is the forward transfer function:

$G(s)=\frac{K_\phi \cdot K_{VCO} \cdot Z(s)}{s}$. Optimizing the PLL noise bandwidth means minimizing the following integral for each noise path through the PLL:

$$\int_{f_1}^{f_2} S_N(f) \cdot |T(f)|^2 df \qquad \textit{Equation 4}$$

$S_N(f)$ represents the specific noise source PSD and T*(f)* the noise transfer function.. Using the approximations for T*(f)* from ***Table 2*** gives us guidance for choosing the PLL parameters that optimize noise performance:

- Maximize the phase comparator charge pump gain (K_ϕ) to minimize the noise contribution of the phase detector (up to a point).
- The N-divider and R-divider noise contributions are proportional to the value of N^2. Choose a phase comparator frequency that results in the smallest possible integer value for N, subject to the maximum phase detector frequency.
- Choose a low noise reference oscillator at the compare frequency, or an integer multiple of the compare frequency. A multiple of the compare frequency provides additional benefit by reducing reference noise.
- Designing the loop filter to have a phase margin of approximately 80 degrees flattens its response and suppresses VCO noise near the loop bandwidth.

The final task is to design the loop transfer function T*(f)* subject to minimizing ***Equation (4)*** for each noise source, which is extremely difficult without the aid of automated tools. National's Web-based design environment WEBENCH® features its EasyPLL tool that assists the user in selecting a PLL/VCO, entering design parameters, selecting loop components, and running simulations to test the design.

Using EasyPLL, a 1.5 GHz sample clock was designed using the LMX2531LQ1500E and a 60 MHz crystal oscillator as a reference, with the following final design parameters:

F_{OSC} = 60 MHz, with phase noise = -158 dBc at 10 kHz offset.

Compare frequency = 30 MHz, R = 2, N = 50

2nd order loop filter, C1= 220 pF, C2 = 150 nF, R2 = 1.0 k Ω, C3=C4=R3=R4=0.

Loop bandwidth = 22.85 kHz

K_ϕ = 1.26 mA

These values resulted in a clock with only 401 fs of jitter (100 Hz to 20 MHz bandwidth). From ***Table 1*** this would give an SNR of approximately 47.6 dB at 748 MHz. ***Figure 2*** shows the single-sideband phase noise plot of the clock. ■

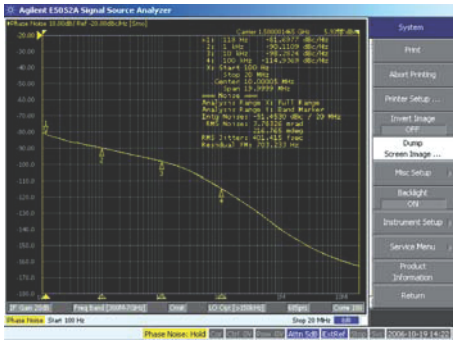

Figure 2. Single-Sided Phase Noise Plot of a 1.5 GHz ADC Clock

For Additional Design Information

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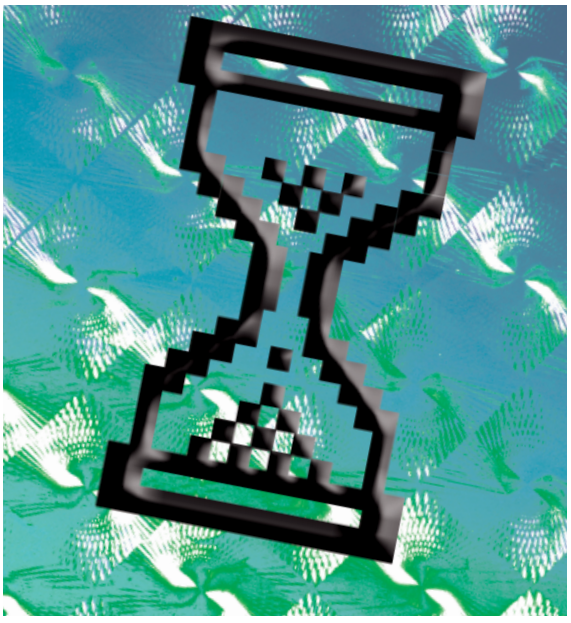

DESPITE GOOD TOOLS, SUCCESSFUL TIMING CLOSURE IS STILL A MATTER OF METHODOLOGY AND ATTENTION.

Timing is everything in SOC design

BY RON WILSON • EXECUTIVE EDITOR

It is a recurring nightmare. The SOC (system-on-chip) design has gone smoothly from day one. RTL (register-transfer level) for each block came in on schedule. Synthesis proceeded with hardly a glitch. Functional verification even ran smoothly. Placement and routing went without incident. And now, the postextraction-timing report is back—with 75,000 failed nets. You sit up in bed, cold sweat on your brow.

For too many designers, this scenario isn't a dream; it is reliving yesterday afternoon. Despite a proliferation of timing-analysis tools, despite the profound assurances of all the IP (intellectual-property) vendors, and despite margins so large they threatened the target operating frequency, what should have been the end of a design project breaks into a frenzy of iterations, Band-Aids, and compromises to resolve massive numbers of last-minute timing faults.

Are the tools to blame? Are the timing models wrong? Why, in an industry that is taking on far more complex challenges—such as optical-proximity correction, design for manufacturing, and process-variation compensation—are we still having trouble just achieving timing closure? And why does achieving it so often cost us too much in area, power, and schedule delay?

EDN sought answers from a number of high-volume ASIC-design shops and some specialized design teams. We heard a number of reasons that timing closure is still hard—and getting harder. But we also heard a reassuring message—that, with best practices, continuous attention, and a focus on timing that begins at project inception, closure can become an almost-routine, predictable part of the design schedule.

THE NEW ISSUES

It's not that closure is getting any easier. "As we have moved into 65 nm, we have been having more challenges with timing closure," says Behrooz Abdi, senior vice president and general manager at Qualcomm. "I think this was probably simply due to the increased complexity of our designs at 65 nm, but we haven't gone back to separate out individual causes."

Even without the growth in complexity, plenty of new issues have added to the problem. An obvious one is higher speeds. But a less obvious facet of that issue is that the high speeds don't always occur in the core of the chip. "One of the most difficult problems we encounter is timing closure on high-speed I/O pins," relates Hao Nham, vice president and general manager of design services at eSilicon. "Today's place-and-route tools just won't do a good job on these high-speed signals without very careful scripting."

Another issue that most design teams must contend with today is the use of third-party IP. Setting aside the whole issue of whether third-party IP arrives in working condition, and it usually doesn't, achieving timing closure within IP blocks is a serious challenge. Documentation may be insufficient for you to even understand the structure of the block without reverse-engineering it. "Often, you have to negotiate hard with the IP vendor just to get enough information to use the block successfully," states Richard Tobias, who at the time of the interview was vice president of engineering at Pixelworks. "You do code reviews and as much due diligence as you can. Then, you go in and fix the IP." Even if repair isn't an issue, the vendor may have based the timing information it provides on switch settings or assumptions about the application entirely different from those they used in this design.

Other kinds of IP have a way of intruding into the timing process, as well.

The most common of these is scan, or its relative on steroids, BIST (built-in self-test). Tools that automatically insert scan chains are generally respectful of timing requirements, but BIST blocks are much larger and more complex, and, necessarily, they have the potential to more greatly disrupt timing. They not only insert devices into signal paths, but also require their own real estate, altering the floorplan and the routing distances between blocks.

"It's not unusual now for an SOC to have 2000 or 3000 instances of RAMs," observes R Chandramouli, product-marketing manager for physical IP at ARM's Artisan Components group. "With their BIST circuitry, self-repair circuitry, and controllers, all those RAMs can cause big problems with circuit complexity and routing congestion. Timing closure becomes a big issue."

But one of the biggest headaches for timing closure may be just emerging as a design trend: the aggressive pursuit of power management. By employing independent voltage islands, dynamically variable supply voltages, dynamic threshold control, and other such techniques, power-management engineers are multiplying—sometimes exponentially—the number of corners that require inspection in the timing analysis. Just identifying the real corner cases in an SOC that has a dozen voltage islands, each of which can operate at any of four voltages, is the stuff of chronic insomnia. Running all the cases is a job for a Google-sized server ranch.

BEST PRACTICES

Yes, timing closure is a hard job. And yes, new design concepts are making it harder. But experienced design managers say that you can tame timing closure by applying best practices in a continuously iterative process that begins at the project inception and continues until sign-off. Far from being a discrete step in the design flow or, worse yet, an afterthought, timing closure has become the heartbeat of a design cycle (**Figure 1**).

Managers describe a simple iteration: Reduce the design to a lower level of abstraction, estimate timing as precisely as possible based on that level of abstraction, set margins to minimize failing nets, fix the outlying nets, and repeat.

"The object is to set your methodology to minimize the number of iterations and to iterate as early in the design cycle as possible," says eSilicon's Nham. If you just set the margins wide enough, it would be possible to ensure at the netlist level that there would be no nets with negative slack in the postextraction analysis. That would save a lot of time. But it would also have dire implications for the overall design: You would be leaving a lot of either performance or energy efficiency on the cutting-room floor. So the iterative process begins even before architectural design, with predesign planning.

"We use a pyramid to describe our timing-closure strategy," explains Jay Jayaprakash, ASIC-design manager at Open-Silicon. "Say we try to get closure on 90% of the paths by pessimism, 9% through analysis, and 1% through actively fixing paths. But if the circuit is very complex, 1% could be 10,000 paths. So, we look at increasing our level of pessimism and the energy we put into analysis until maybe we are fixing only 0.1% of paths. But that may cost too much power. Even in the best methodology, you have to learn to be efficient in dealing with that last fraction of the paths. You have to agree on a strategy with your customer."

AT A GLANCE

- Despite tools and years of practice, timing closure continues to be a major issue in chip design.
- Only a methodology that continuously refines timing estimates and deals with failing paths throughout the design flow can cope with the problem.
- The strategy is to make iterations as early as possible and to leverage the skill of experienced physical-design experts.
- New design techniques to enhance speed or reduce power also complicate timing closure.

THE FIRST STEPS

"First, understand the design requirements," Nham advises. In other words, have a clear agreement with the customer on the acceptable windows for die area, performance, active and standby power, choice of process technology, and design schedule. All of these things can trade off against each other. For instance, a design team can meet an impossible-looking schedule if you relax all the other constraints, allowing virtually a push-the-buttons design flow. Or, the team can hit a very challenging speed target if it has unlimited area and power for dealing with slow paths and extra schedule for combing through them. The critical point is not to get locked into a set of requirements that will force tight margining on both timing and power and leave no resources to deal with the plethora of timing violations these choices will produce.

Once you've settled the design goals—always subject to later renegotiation, unfortunately—the focus of timing closure moves to architectural design. Choices that the chip architect makes can significantly influence the ease of achieving closure by determining the necessary operating frequency and hence the timing budget between stages.

Decisions such as whether to use a single fast CPU core or multiple slower cores, for example, can have a significant impact on operating frequency. In a recent mobile media-processing SOC that 3Dlabs designed, the choice of a pair of ARM926EJ cores over a single ARM11 meant that the cores could operate at a maximum of 200 MHz and meet all task deadlines. The fact that numerically intensive processing is done on a 24-element processing array meant that the array could run at no more than 100 MHz—a small fraction of the clock frequency that would have been necessary for a typical single-instruction, multiple-data coprocessor.

More subtle architectural decisions are important, as well. How deeply can the design pipeline processing units? Can you organize state machines so that the fastest state transitions are highly localized? Can you organize memory blocks to limit the physical distance between a client and the memory it must access? All of these decisions can remove—or generate—critical timing paths simply by changing the delay budget available for them.

Floorplanning also plays a vital role here. There are obvious issues, such as putting SERDES (serializer/deserializer) blocks close to high-speed I/O pins. And there are less obvious and more time-consuming steps, such as hand-placing smaller memory instances.

"It's not uncommon to have a few hundred memory instances in a design," eSilicon's Nham says. "It's best if skilled

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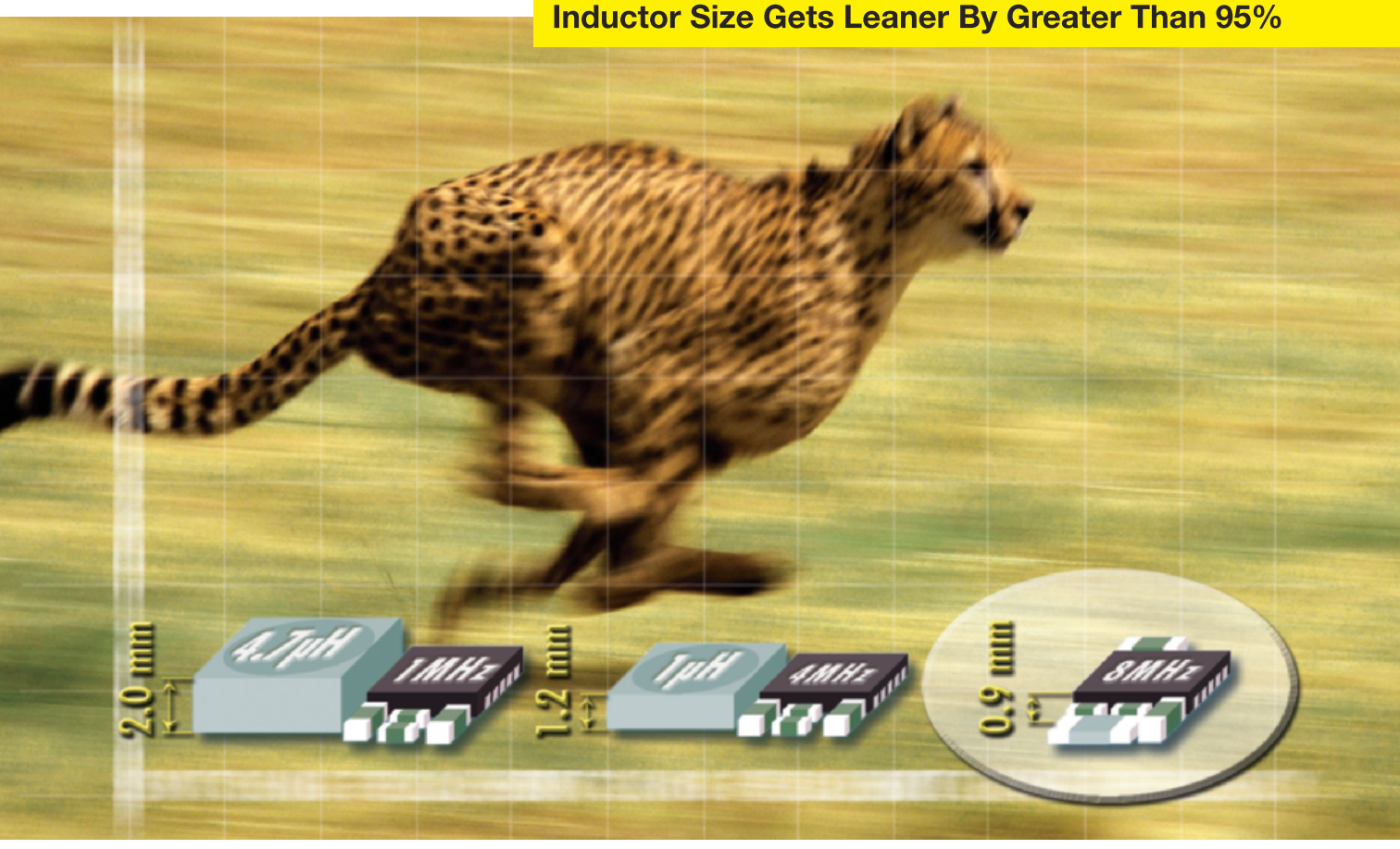

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designers place these instances in the floor map. That way, you can get pretty accurate estimates of the timing through the memories very early on." These steps take place before RTL code even exists for much of the design, yet they can significantly impact closure later on.

BEGINNING WITH RTL

Detailed RTL coding of individual blocks is perhaps the place at which designers begin to think seriously about timing issues. As we have seen, this point is much too late to start. But contributions to the timing-closure process get more frequent and more obvious from here on out.

The literature on RTL styles, best practices, and tricks to influence timing closure is large and too detailed to review here. Physical-synthesis tools have subsumed many of these details, so that the designer's control over the RTL optimization for timing is almost entirely through constraint files and synthesis directives. Interestingly, this approach puts a premium not on logic-design skill but on understanding the workings of the synthesis tool.

Some experienced designers recommend keeping constraints as simple and slack as possible. Doing so reduces the runtime for physical synthesis, of course.

STATISTICAL ANALYSIS TAKES ON TIMING VARIATIONS

Identifying corners for timing analysis has always taken process variability into account. But at 90 nm and below, process variation doesn't contribute one variable to the timing problem; it contributes many. Variations may occur not only in the effective channel length, but also in channel mobility, threshold voltage, contact and via resistance, metal dimensions, and other areas. Including each of these important sources of variation in the selection of process corners for timing analysis would produce dozens or hundreds of corners.

Equally problematic, such analyses would be too conservative. Many of the variations are relatively uniform throughout a single die or a wafer. (These variations are die-to-die.) Others are random in nature and tend to average out, rather than accumulate, along a path. So, corner-based analysis may establish margins that are far larger than they need to be, because corner-based analysis assumes that all parameters are simultaneously at their worst-case corners–an extremely unlikely event in reality.

The literature has identified statistical-timing analysis as a way to attack this problem. But moving from identification to a production tool is another matter entirely. One vendor that has achieved this goal–albeit only with internal designs and a few technically very strong customers, is IBM (Figure A).

"The basic principle is to do the analysis from just one corner," explains Leon Stok, director of EDA in the Systems and Technology Group at IBM. "We analyze variations from this one corner to see whether timing margins improve or get worse in each process-parameter dimension, such as voltage and metal tracking."

"This statistical tool is applied primarily in sign-off," Stok continues. "It is embedded in [IBM's] EinsTimer [statistical-timing-analysis tool], so it becomes just another part of the sign-off process. In practice, the designers get a timing-slack report just as they ordinarily would. It shows the paths with negative slack, and also paths with positive slack that the tool still considered to be critical. The difference from conventional static-timing tools is that the designer also gets a statistical report on the sensitivity that each of these paths has to the specific factors we are tracking.

"Internally, we set margins so that the user doesn't have to deal with a ridiculous number of paths in the report. The margins, like the sensitivity analysis, are based on the statistical data we have collected from test wafers and from test patterns on production wafers. In addition to eliminating paths that are going to have positive slack, we provide a fix-up tool–an incremental routing, buffering, and sizing tool–that works with the statistical timer. That [tool] should reduce the typical report from maybe 10,000 initial paths to a few hundred that the designers will actually have to examine. And we provide training so that the designers will understand how to interpret the sensitivity data they are getting.

"Overall, the statistical approach removes a certain amount of unrealistic pessimism from the timing analysis. That means having to look at fewer nets and wasting less time, power, and space on overdesign to meet unnecessarily wide margins."

Stok says that IBM's flow provides timing information at each level of abstraction in the design flow. But the statistical tool comes in at the end, when there is enough physical-design data for it to discriminate between necessary guardbands and unnecessary pessimism.

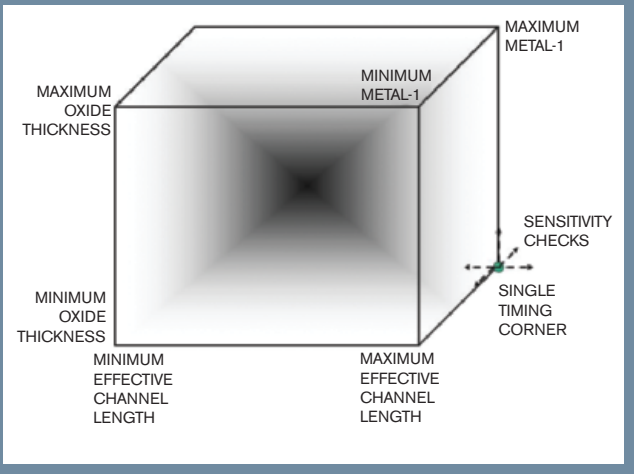

Figure A IBM's statistical timing approach starts from one process point and computes sensitivities, rather than performing analysis at all possible corners.

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DAC082S085	8-bit	2	3 µsec	MSOP-10, LLP-10
DAC102S085	10-bit	2	4.5 µsec	MSOP-10, LLP-10
DAC122S085	12-bit	2	6 µsec	MSOP-10, LLP-10
DAC084S085	8-bit	4	3 µsec	MSOP-10, LLP-10
DAC104S085	10-bit	4	4.5 µsec	MSOP-10, LLP-10
DAC124S085	12-bit	4	6 µsec	MSOP-10, LLP-10

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But it also avoids complex iterations of the synthesis step, with modifications to the constraints on each iteration. The problems are not only the time consumed, but also the difficulty in capturing and tracking the changes in the constraints so that you can reproduce the design if it needs RTL changes later in the cycle. The synthesis tool will do whatever it can think of to meet timing constraints, often at a direct cost in area and power. Later changes in logic design, without closely examining the constraints, can produce interesting results—in the negative sense of the word.

Needless to say, a thorough look at the netlist-timing analysis is vital, even though the estimates are still not based on physical data. It is at this point at which Jayaprakash's pyramid sets its base. The pessimism that Open-Silicon counts on to remove 90% of the timing failures begins with the largest possible margins on netlist-timing estimates. "We ask our customers to give us a substantial timing margin at this point," Jayaprakash says. "The industry average is about 15 to 25% using zero-wire-load models." As always, there is a trade-off that you must base on the customer's design requirements. If the chip has to be near the physical-speed capabilities of the chosen process, a large margin at this point will simply cause lots of synthesis iterations, as the tool tries everything before giving up. But too small a margin may substantially increase the number of postplacement failed paths, as the discrepancies between the physical-synthesis tool's timing guesses and the placement-based timing guesses exceed the margins.

Designers will also be inserting test structures into the logic now—BIST structures during RTL development or after first synthesis, and scan structures after logical synthesis. It is important to remember that none of these structures are transparent to signal timing.

But there is another issue with BIST structures, as well. BIST will introduce into the design new operating modes that must have their own timing analysis. Often, they will involve both paths that are not used during normal operation and different frequencies. (This consideration will resurface with a vengeance after physical design.)

It's at this point, after synthesis but before detailed placement and routing,

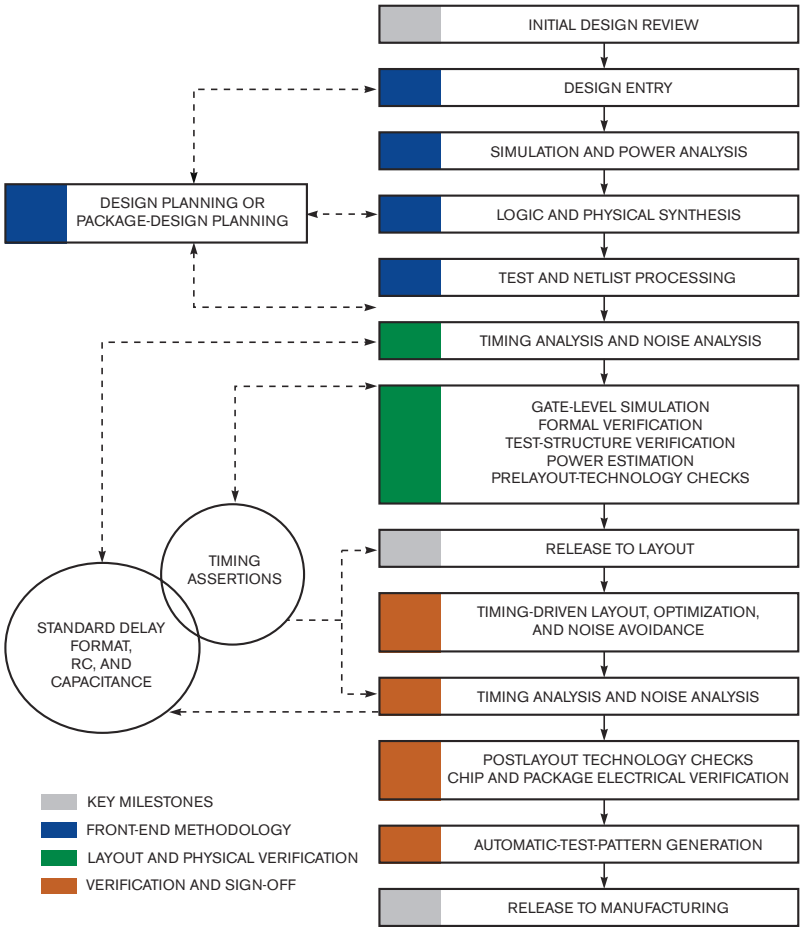

Figure 1 This example of an IBM ASIC flow shows multiple points for timing checks in both the front end and the sign-off process.

that experience may have the greatest leverage on successful timing closure. Both Jayaprakash and Nham emphasize the importance of having previously taken similar blocks through the full design cycle.

"You can't always even identify the critical paths at the netlist level," Nham says. "But you can intuitively spot problem design areas, see where constraints are missing, and do other reality checks on the netlist timing. It's a matter of interpreting the tool output based on your experience with previous similar blocks—categorizing the block design and setting synthesis parameters based on what has worked with similar designs in the past. If you get the right tool parameters, you'll get timing closure."

Jayaprakash agrees: "We match the style of a particular block against the other blocks we've done in our 50-some previous designs and adjust the timing margins based on how much margin we have needed in the past on similar blocks." This approach, coupled with the ability of tools to give feedback on timing in a matter of hours for a whole region of the chip, makes iterations at the netlist level to cleanse timing paths a powerful method.

PLACEMENT AND ROUTING

During the placement-and-routing process, more detailed models built on increasing amounts of real physical data replace the rough fan-out-and-pattern-based models of the synthesis phase. As in previous steps, there is always the trade-off between accepting more failed paths and asking the tool to try harder. But, at this point, manual intervention becomes an important factor, as well.

In the most complex designs, says Open-Silicon's Jayaprakash, even if you have succeeded in getting 99.9% of the

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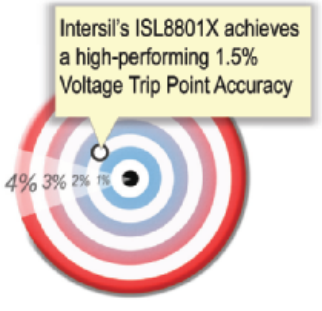

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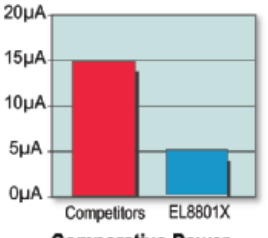

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nets to pass, you still have thousands of failed paths. The first response to this report might be to crank down on the constraints and run the tools again.

"Don't just keep pushing the button," Jayaprakash urges. "The first step should be to ask why the tools didn't fix the timing violation in the first place. If you could look at each failed path, you might see obvious things. A flip-flop has violations on both input and output, so the tool fixed only one. Maybe all the paths into a memory are failing because the memory is just in the wrong place and you didn't allow the tool to move it. Maybe there's a problem with one widely used clock."

Nham observes that hold-time violations are particular problems. "The tools don't deal well with them today," he says. "They tend to fix the setup violations and not the hold violations."

Open-Silicon uses scripts that categorize the failed paths according to starting and ending points, clock sources, physical region, and a number of other parameters. The resulting spreadsheet allows designers to sort failures into maybe 15 buckets, for which all the paths in a bucket are likely to have similar causes of failure. "Now, 10,000 violations become a manageable 15 buckets," Jayaprakash says. Experienced designers can then go through the buckets and identify the large-scale issues.

After you have completed this task, there will still be some number of paths, probably in the low hundreds, that are one-off issues. But this problem is manageable.

With simpler chips, the process is similar, but the scale is smaller. "If you have been eliminating violations from the netlist level on, you should be left with dozens, not hundreds, by physical-design time," Nham says. "This is important, because, if you are trying to fix hundreds of violations all at once, the odds are that you will inject new violations as you fix the old ones. Even with a small number of violations, though, there is no tool that can substitute for an experienced layout engineer at this point."

Two more analyses intrude here to complicate the problem: signal integrity and IR drop. After all the unpleasant timing surprises that the routing and extraction tools reveal, these two additional tools have their own bad news to bring. Signal-integrity tools may demand additional delay on victim nets to allow coupled transients to settle. And IR-drop analysis may tell you that your drive strength is not what you thought it was.

"Once you get up to a few million gates, you have to do IR-drop analysis," opines Jayaprakash. "It serves a number of purposes. It is necessary when design constraints are tight. It can be used in the final analysis pass to prove the existence of critical vias—which layout-versus-schematic analysis will not do, by the way."

IR-drop analysis estimates the actual load at each node in the supply network and then estimates the resistive loss through the supply network and, hence, the actual supply voltage on the device driving each signal node. It requires an accurate model of the supply-trace resistances and—more critically—an accurate estimate of toggle rates in all the operating and test modes. Often, the design team will have to estimate the toggle rates and then feed the information back to architects for validation. The tool will report a problem as an additional delay on a path due to the lower drive strength.

But it gets worse. "At 90 nm, you need to do both static- and dynamic-IR analysis," Jayaprakash warns. "The static analysis may look fine, but you can have V_{DD} drop by a factor of two for a tenth of a cycle. That's a killer." The

FOR DRAM, TIMING CLOSURE IS A DIFFERENT GAME

According to Qimonda principal engineer for DRAM-product development Thomas Vogelsang, timing closure for a new DRAM design is every bit the challenge that it would be for a new SOC (system on chip). But the process is profoundly different.

Three factors make the difference, Vogelsang suggests. First, key parts of a DRAM are asynchronous, and some of them are purely analog rather than digital. This situation brings a whole new set of tools into play. Second, DRAM development is an evolutionary process, so that each new design builds upon a long history, giving designers a lot of experience upon which to rely when making timing estimates early in the design cycle. Finally, timing closure in DRAM occurs from the bottom up, rather than the top down.

"The most critical part of timing analysis for DRAMs is parasitic estimation," explains Qimonda director of DRAM-product development Michael Kleiner. Vogelsang adds that parasitics account for a large part of the total timing budget for a cycle. This situation means that final analysis starts at the most physical level, with patterns of polygons that occur in the memory array. Field solvers create parasitic models for these polygon patterns, which are then put into a table.

Then, a pattern-matching tool scans the physical design of the array, matching patterns it encounters with patterns in the table and extracting the appropriate parasitic values. This approach leads to an overall Spice model of drive transistors and parasitics for the array. The Spice simulation has to cover known process corners, as well as IR drop, and follows signals into the array, through the memory cells, and out through the sense amplifiers. This method leads to timing values for the memory array itself, derived not from estimated delay figures but from simulation waveforms.

Designers then combine these values with traditional static-timing analysis and FastMOS simulation runs on the synchronous-digital-control and interface logic to produce an analysis of the overall chip. Finally, designers employ Monte Carlo analysis on the I/O pins to derive a full picture of the pin-to-pin timing of the device.

As DRAMs become more complex, the balance is gradually shifting toward static analysis, Vogelsang says. "DDR-3, for example, is a much more complex design, with many more clock cycles per operation. So, static-timing analysis becomes more important." But nothing changes the fact that the heart of the chip, and the source of most of its delay, is an array of very analog circuits.

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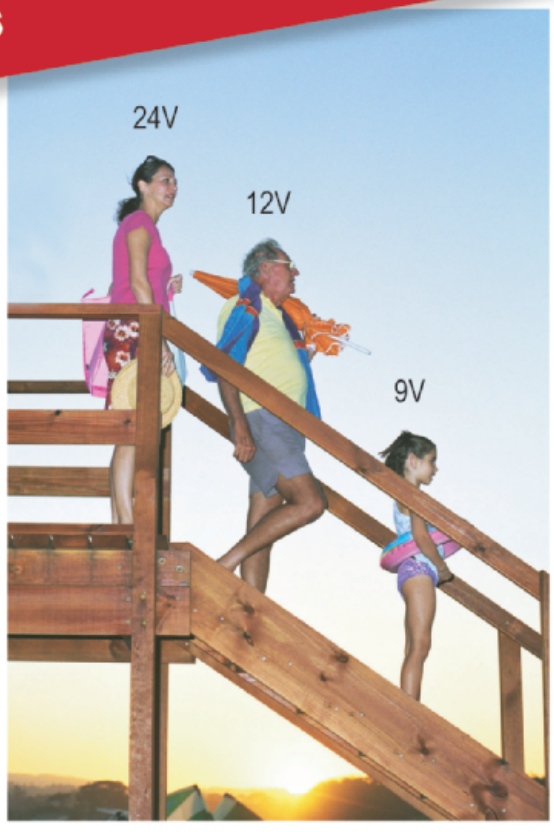

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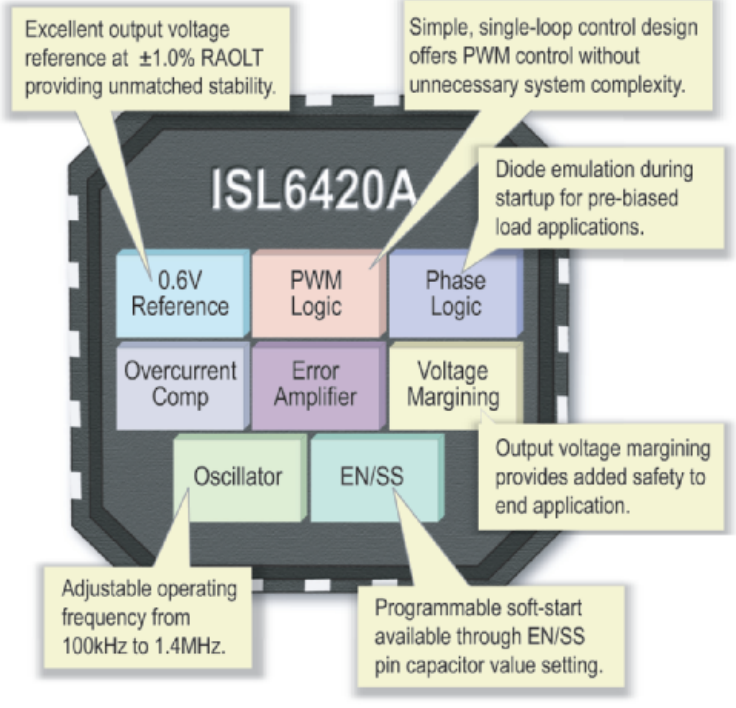

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solution is usually using any available space in the interconnect stack to hide decoupling capacitors.

At this point in the design flow, careful analysis of test modes—especially for BIST structures—is vital. "The scan mode may use a much lower frequency, so at first glance it works fine," Jayaprakash observes. "But it may have a 50% toggle ratio—far above anything that is reasonable in normal operation. You have to analyze it separately, with its own toggle rates."

As architects and designers struggle with the challenges of extreme processes and power constraints, they are unintentionally compounding the problems of timing closure. One example is the growing issue of process variations. The less reliable early predictions of timing are, the wider the margins have to be. Add in process variations that can change interconnect-line widths or transistor-drive currents by a factor of two, and the margins have to be so large that many designs become impossible on paper. Statistical static-timing analysis is one way to attack this problem (see **sidebars** "Statistical analysis takes on timing variations" and "For DRAM, timing closure is a different game").

But a seemingly more innocuous design trend may turn out to be a bigger issue. The use of independent voltage islands and dynamically adjustable supply voltages—along with the use of dynamic threshold voltages—threatens to become a huge issue.

Just defining the islands and correctly inserting the level shifters can be the first problem. "The tools still need improvement in dealing with voltage islands," eSilicon's Nham warns. "Insertion of the interface cells isn't as fully automatic as it's supposed to be. And errors in inserting them lead to soft errors in the chip."

A more intractable problem is the sheer number of corners created by a design in which each of a half-dozen voltage islands may, at any given time, be operating at any of five voltages. "We employed a number of voltage islands in our portable media-processing architecture," reports Nick Murphy, vice president of architecture at 3Dlabs. "Because of that [step], the number of timing corners grew enormously. The big problem turned out to be unexpected hold violations. It turns out that path delays vary unevenly with changes in supply voltage, so it is not safe to make simplifying assumptions about how the timing relationships change when you turn the voltage down. We ended up developing our own sign-off procedure for the chip."

Open-Silicon's Jayaprakash recommends using the following strategy to try to beat this problem: "Running corners at 11 voltage modes is infeasible. So, we try to identify worst-case modes, high speed and low speed, and just use those corners."

But, if the future brings new problems, it is also bringing new solutions. Several IP companies now offer versions of GALS (globally asynchronous, locally synchronous) interconnect technology. By making all of the paths between blocks self-timed, or, in some cases, timing them to a much slower master clock, the hope is to eliminate timing closure for the long wires that are the chronic sources of trouble in final timing closure. This step, in effect, pushes timing closure down in the hierarchy until it is necessary at only the block level.

Carrying this concept to its extreme, you can make critical paths within blocks self-timed, as well. In fact, this practice is already common in some companies that have the resources for custom-design work. And wholly self-timed chips (out to the external interfaces)—notably an ARM processor and a family of interconnect switches—are on the market today. This approach may, as process issues continue to grow, be the future: a time when timing closure will be a specialized method applying only to certain legacy-circuit designs. In some ways, it would be a relief. **EDN**

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CONTINUOUS TECHNOLOGICAL EVOLUTION IS THE INEVITABLE CONSEQUENCE OF VENDORS' DESIRES TO SUSTAIN REVENUE AND PROFIT AT HEALTHY LEVELS. WHEN THAT PRODUCT PROGRESSION RESULTS IN REGRESSIVE EXPERIENCES FOR END USERS, HOWEVER, ITS SUSTAINABILITY IS UNCERTAIN.

CONNECTING SYSTEMS TO DISPLAYS: WHAT WE GOT HERE IS FAILURE TO COMMUNICATE

Peer at the back of a modern home-theater receiver, and you'll note a preponderance of analog-signal-carrying connectors amid the plethora of plugs (**Figure 1**). RCA jacks route low-level analog-audio signals, and banana plugs and binding posts handle postamplification connections to speakers. RCA jacks also tackle video duties: one for each composite-video output and three for each higher-quality-component video bus, with S-Video an intermediary-quality and -complexity option (**Reference 1**). RGB video comes in a variety of plug flavors: RCA, RF, and nine- and 15-pin versions, along with a variety of more proprietary alternatives.

Peer closely at the bottom two rows of the AVR-5805 back panel, however, and you'll notice that Denon is also embracing the digital-audio future. RCA jacks can also handle S/PDIF (Sony/Philips digital-interface) bit streams, as can optical-fiber plugs. Both proprietary Denon Link and industry-standard Ethernet RJ-45 interconnects tackle networked audio, as does IEEE-1394—that is, FireWire (**Reference 2**). Wires are no longer absolutely necessary, of course; a burgeoning number of wireless schemes are also contending for your next-generation design consideration (see **sidebar** "More at EDN.com"). And, for video, direct your attention to the DVI (Digital Visual Interface) and HDMI (high-definition-multimedia-interface) plugs on the receiver back panel's top row.

Before reading more about DVI and HDMI, first consider a "bigger picture" question: Why is the analog-to-digital conversion happening? The answer begins with multimedia sources; audio historically has come from cassette tapes and LP records, but its primary starting places nowadays are optical discs and both downloaded and streamed varieties of Internet-housed bi-

nary files (**references 3** and **4**). Optical discs, along with digital bit streams over terrestrial antenna, cable, DSL (digital-subscriber-line), and satellite links, are also common video sources, and all of them replace earlier generation content, such as analog broadcasts and videotapes (**Reference 5**).

Next, look at the other end of the distribution chain, the last step or few before the content reaches your eyes and ears. The processes that generate sound waves and photons are inherently analog, but, for audio, *EDN* has extensively covered the emergence of Class D digital amplifiers for driving the transducers (**Reference 6**). And, for video, digital-centric alternatives, such as DLP (digital-light-processing), LCD, LCOS (liquid-crystal-on-silicon), and plasma technology are replacing analog CRTs, which are fading from prominence (**references 7** and **8**).

Now, consider the multistep process that audio and video traverse between their source and their destination. Digital-domain processing—resampling, resizing, mixing, format transcoding, and other tasks—can by itself induce potentially detectable quality-degrading transformations to your system's multimedia material. Eliminating unnecessary *additional* digital-to-analog and analog-to-digital conversions not only potentially reduces system cost, but also keeps the source content in as pristine condition as possible before reaching its ultimate endpoint: you. Analog content is also subject to degradation from its transmission medium, due to such factors as cable-impedance attenuation and imperfect load-impedance matching, and from its operating environment due to EMI coupling. And it's difficult to multiplex multiple analog signals on a single wire in an interference-free fashion; the multiplexing process is simpler in the digital domain.

One other important digital "advantage," at least to some folks, bears mentioning: Media-content rights-holders have struggled for years and are still struggling to copy-protect analog content, most notably through technologies such as Macrovision. Digital-domain material is much more straightforward to encrypt. This lockdown plugs the perceived Achilles' heel interconnection between video source and display, thereby controlling such factors as who accesses it, how many times they can access it, how long they have to first access it and how long thereafter, with what quality they can listen to and view it, and whether they can make a copy of it and, if so, how many copies and with what quality level.

DRM (digital-rights management) also more readily lends itself to several ideal characteristics of a content-control system: renewability, revocability, and upgradability (**Reference 9**). And, when DRM breaches inevitably occur, digital-domain watermarking identifies the source of the infringement, speeding prosecution. Yet, as you'll see as you read on, DRM flaws are at the root of the problems many end users have when they try to use modern consumer-electronics devices. When a digital-interconnect scheme not only results in restricted media access compared with its "fair-use" analog predecessor, but also spawns more usage glitches than this precursor, consumer backlash is inevitable.

AT A GLANCE

- Digital interfaces deliver numerous potential advantages over analog predecessors.
- Content owners extol DRM (digital-rights management); end users are less enthusiastic about it.
- DVI (Digital Visual Interface) was in many respects ahead of its time and has not displaced analog connections to the degree that its developers originally envisioned.
- HDMI (high-definition multimedia interface), a DVI descendant, has achieved widespread adoption, fueled by the large amount of multimedia content end users consume in living rooms and the perceived need for DRM of that content.
- DisplayPort has so far been an underperformer, but Intel's rumored support may yet jump-start it.

DVI: THE DIGITAL DEBUTANTE

When Intel announced the formation of the DDWG (Digital Display Working Group) at the fall 1998 Developer Forum, the company put the stamp of approval on an interface technology, DVI, which Silicon Image had been promoting for several years as the TMDS (transition-minimized-differential-signaling)-based PanelLink topology. At the time, DVI wasn't the only game in town; in fact, the VESA (Video Electronics Standards Association) was championing two other TMDS-based approaches: P&D (plug and display) and DFP (digital flat panel). Apple's ADC (Apple Display Connector) was also TMDS-derived, but the connector and cabling additionally carried USB and display power buses. National

Figure 1 The bewildering array of back-panel connectors on this Denon receiver illustrates the appeal of digital-enabled consolidation.

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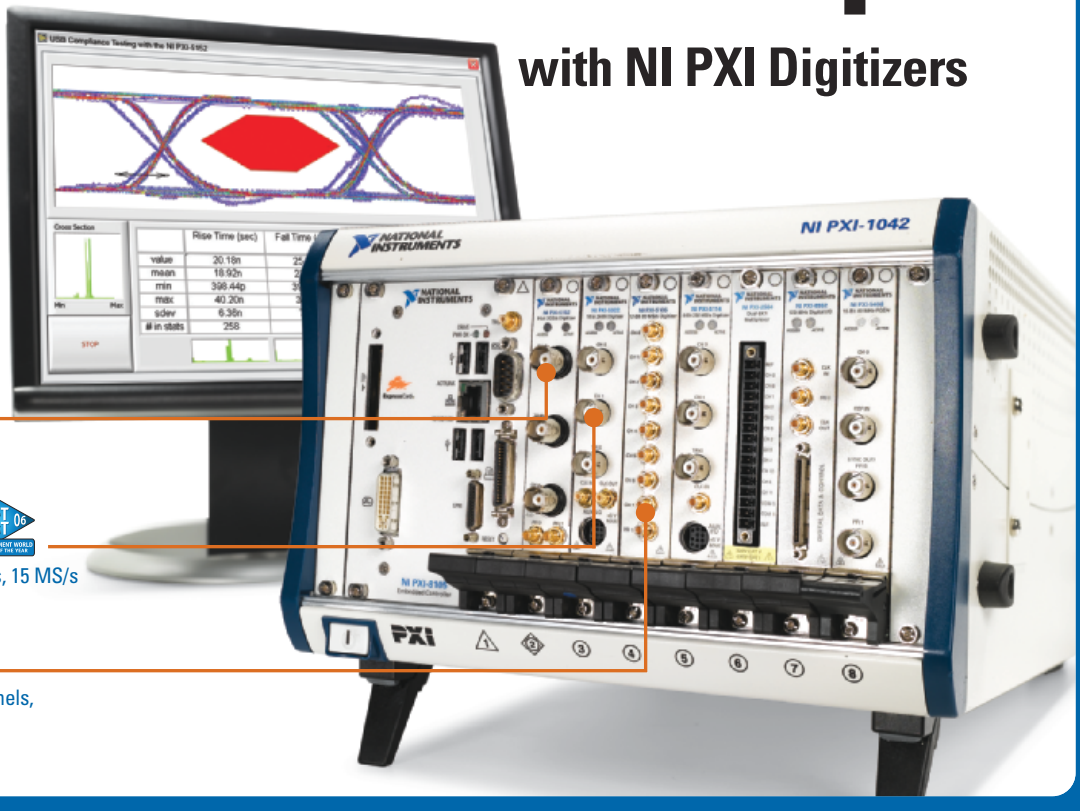

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Semiconductor championed another notable contender, OpenLDI (Open LVDS Display Interface), a fact that's probably not surprising to those of you who know of the company's long involvement with LVDS (low-voltage differential signaling).

Intel's influential blessing swung industry momentum in DVI's direction, however, and the alternative approaches faded from prominence. OpenLDI, for example, saw its most visible success with Silicon Graphics' 1600SW LCD, which touted then-leading-edge features, such as a 17-in.-wide screen, 1600×1024-pixel resolution, a 350-to-1 contrast ratio, and a 0.23-mm (110-dpi) dot pitch. However, only three graphics cards, from 3Dlabs, Formac, and now-defunct Number Nine, natively supported its OpenLDI interconnect. Out of necessity, SGI developed a MultiLink adapter that translated OpenLDI to the more common VGA (analog) and DVI (digital) protocols. And, whereas P&D was conceptually similar to DVI, VESA attempted to comprehend not only analog and digital video, but also USB and IEEE 1394 (FireWire)-tethered peripherals, such as mice, keyboards, printers, and audio devices. The DDWG instead used this additional connector real estate to implement an optional second parallel DVI link, thereby supporting higher resolution displays.

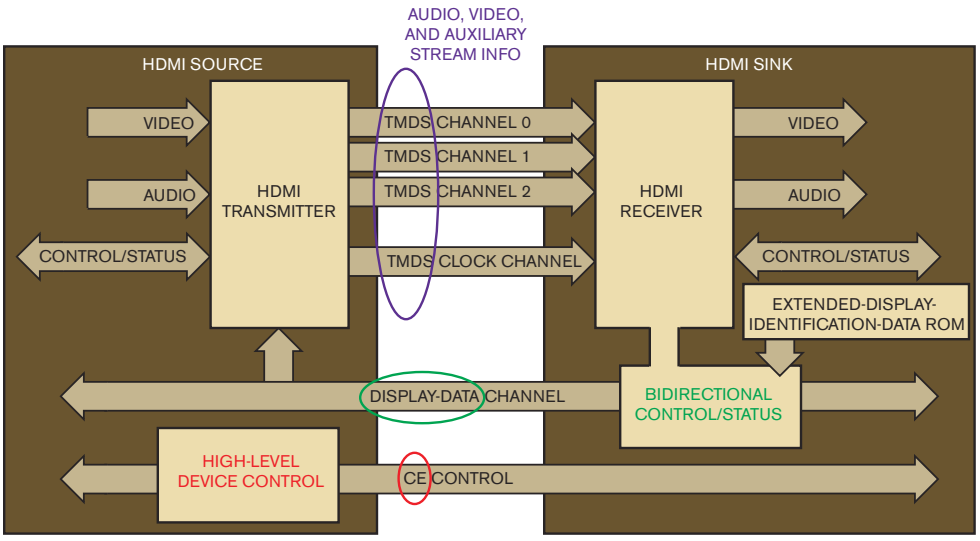

Figure 2 DVI dedicates a twisted-pair link to red, green, blue, and clock signals; the HDMI follow-on incorporates support for audio, remote control, and other enhancements.

At the time it unveiled its support of DVI, Intel had a long and generally successful legacy of driving de facto standards, such as PCI (Peripheral Component Interconnect) and PCMCIA (Personal Computer Memory Card International Association), into the marketplace. Rigid compliance testing and periodic industry "plugfests" were key factors in that success.

TABLE 1 HDMI ITERATIONS

Specification version	Release date	Additions
1.0	December 2002	Initial release
1.1	June 2004	Added DVD-Audio support
1.2	August 2005	Added SACD (super-audio-compact disc)-support; eliminated connector and RGB-color-space restrictions to satisfy PC-industry needs; required displays to support future low-voltage, ac-coupled sources
1.2a	December 2005	Fully specified the CEC (Consumer Electronics Control) protocol and testing procedures, improved cable and connector testing and verification procedures, established a certified connector list
1.3	June 2006	Higher link bandwidth (thereby enabling features such as higher resolutions, higher frame rates, greater color depths, and an expanded color gamut), transport support for Dolby TrueHD and DTS-HD Master Audio lossless audio formats, support for lip-synch correction, mini connector

However, the development of DVI lacked a similar formal compatibility-validation process, an omission that was to its detriment. (Intel didn't develop DVI and therefore had less control over it, which may partially explain this omission.) DVI runs at a 165-MHz maximum clock speed with a 10-bit-per-clock transfer rate. After comprehending 8B/10B encoding and the eight-wire (four-twisted-pair) bundle per link (red, green, blue, and clock), this clock frequency translates to a peak single-link bandwidth of 3.96 Gbps and peak single-link resolution of 1920×1200 pixels (24-bit color, 60 frames/sec) (**Figure 2**). However, some silicon suppliers, particularly those that attempted to integrate a DVI transceiver within a larger piece of silicon, such as a graphics chip, were unable to meet the 165-MHz design target. (DVI's I^2C-based DDC (display-data-channel) bus is the means by which graphics chips and displays communicate their respective capabilities and limitations to each other.) And neither video-output devices nor displays commonly supported the dual-link DVI implementation, delivering as much as 7.92 Gbps of bandwidth and 2560×1600-pixel resolution.

Design difficulty led to another DVI shortcoming—this one more financial in nature. In exchange for Intel's bless-

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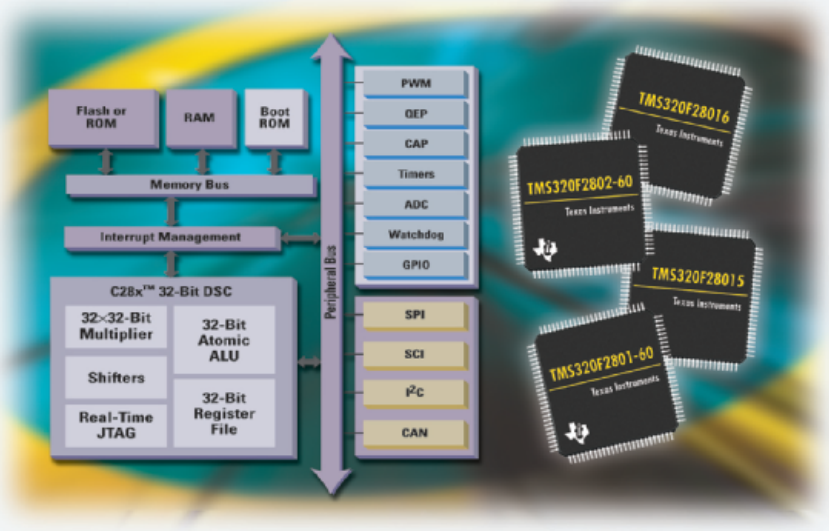

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ing, Silicon Image vowed to offer up its fundamental technology patents in a royalty-free fashion. However, the company retained control over its DVI *implementation* patents, and Silicon Image thereby obtained a lucrative revenue stream not only from other companies that bought its DVI chips, but also from those whose DVI-circuit designs overlapped its own. Adding to the industry angst over DVI was the fact that Intel was an investor in Silicon Image; a portion of Silicon Image's DVI-related income, therefore, ended up bolstering Intel's coffers.

When DVI entered the market, it faced a substantial legacy inventory of VGA-only displays in users' hands. Graphics cards might add DVI support, but, at least in the near term, eliminating VGA capability would mean fiscal suicide. Indicative of this fact, the most common DVI-connector option, DVI-I, incorporated both analog and digital interfaces and, through a dongle, could transform into a legacy 15-pin VGA plug. Intel's early promotional materials for DVI claimed that the computer industry was nearing an inflection point at which burgeoning display resolutions would couple with finer dot pitch to leave analog interfaces incapable of delivering adequate-quality images. Nearly 10 years later, this inflection point largely still hasn't materialized. Out of fairness to Intel, at least some of the reason for the delay is largely out of the company's control; Microsoft's operating systems don't yet robustly implement resolution-independent rendering of GUI elements, such as fonts and icons. (Windows Vista should make significant improvements in this regard.) And these elements on fine-pitch displays are therefore difficult to discern. Silicon suppliers have also made tangible improvements in the SNR, switching speed, and other attributes of their analog-video transmitters and receivers, thereby delaying DVI's ascendancy.

HDMI: AN EVOLVING DERIVATIVE

DVI's connector form factor was adequate for computer applications, but consumer-electronics suppliers needed something smaller and more user-friendly—without screws, for example.

(a)

(b)

Figure 3 Manufacturers judged the DVI connector (a) as too bulky and cumbersome for consumer-electronics usage, prompting the development of the slimmer and simpler HDMI Type A plug (b). HDMI's newest Type C connector is even more svelte, with digital-still-camera and videocamera usage in mind.

Yet you shouldn't view HDMI as simply a shrunken DVI port (**Figure 3**). As its name implies, its developers, chief among them Silicon Image, incorporated in a DVI-backward-compatible manner the ability to transmit both video and eight-channel audio data (compressed and uncompressed, 24-bit sample size, 192-kHz sample rate) down a single cable. (See **Figure 1** to understand the appeal of this enhancement.) Initial HDMI-draft versions modulated the audio information on the clock signal; nowadays, audio-data transfer occurs within "data-island" intervals—that is, during horizontal- and vertical-display blanking periods. HDMI's beyond-the-PC focus also necessitated that it support not only RGB, but also 4:4:4 and 4:2:2 component-video formats. And HDMI supports three encoding protocols: 8B/10B for video that can tolerate an occasional dropped bit, 4B/10B for audio, and 2B/10B for the most critical control information.

Ever since the initial Version 1.0 specification release in December 2002, HDMI has undergone regular enhancements in a backward-compatible manner (**Table 1**). Note, for example, that Version 1.2a formalized support for CEC (Consumer Electronics Control), a remote-control scheme employing the AV Link protocol, whose implementation in HDMI sources and destinations is optional but whose wiring support in cabling is required. The latest HDMI iteration, Version 1.3, increases the maximum single-link clock rate to 340 MHz, an enhancement that will require not only Version 1.3-compliant endpoints on both ends of the HDMI link, but also a Category 2 speed-certified cable for end users to benefit from it. Those benefits, which arrive through 10.2 Gbps of raw bandwidth, including error detection and correction encoding, might alternatively include boosting per-link image resolutions, boosting per-link image-frame rates, and increasing image-color depth beyond 24 bits/pixel. This depth increase would come through HDMI's support for 30-, 36-, and 48-bit—that is 10, 12, and 16 bits/component—color in both RGB and component-video formats.

Another benefit end users would derive from Version 1.3 is an expansion of the image-color gamut through support for the next-generation xvYCC color-space standard. HDMI Version 1.3 also broadens audio-transport support to encompass the latest high-fidelity lossless-compression formats from Dolby Labs and DTS. This addition is significant only if the transmitting device is incapable of decoding these formats; if it can decode these formats, it could alternatively employ the support for uncompressed audio transport in earlier HDMI versions, along with multichannel-analog-audio connections. Lip-synch correction compensates for the differing latencies you incur when processing audio and video throughout the home-theater-equipment chain, and the developers of the miniature Type C connector designed it with multimedia transfers from compact digital still cameras and videocameras in mind.

Skeptics might wonder whether HDMI Version 1.3's higher bandwidth

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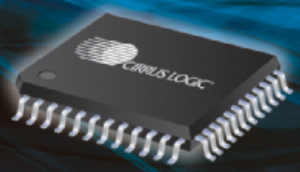

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capabilities are meaningful in real life, because previous HDMI iterations already handle traditional video sources, including standard- and high-definition optical discs and standard- and high-definition television from cable, IPTV (Internet Protocol television), terrestrial, and satellite providers. Three words suffice to respond to that cynicism: cameras, computers, and consoles. The importance that console- and computer-game enthusiasts place on high frame rates, enabling gamers' fast-response aspirations, is indisputable (**Reference 10**). Modern cameras can easily capture high-resolution, HDR (high-dynamic-range) images, and modern computers can easily render and output them. And display innovations, such as deep-black capability, LED backlights, multicolor-backlight arrays, and BrightSide Technologies' impressive per-LED, per-frame control of both white- and multicolor-LED arrays, are increasingly able to deliver these rich images to viewers (**Reference 11**). Displays are no longer handling just traditional video sources, and, with HDMI Version 1.3, the link between system and display is no longer the quality bottleneck.

No discussion of HDMI would be complete without covering DRM. The belief that all HDMI-inclusive devices also implement DRM is a common misconception; in actuality, HDCP (high-bandwidth-digital-content-protection) support is optional, albeit common, in HDMI, just as it was with DVI in the form of DVI-HDCP, and its implementation incurs the payment of additional royalties to HDCP intellectual-property-rights holders. Although the HDMI Founders organization learned from DVI's shortcomings and has implemented a formal validation process, this validation historically has not extended to cover the optional HDCP. As a result, and perhaps not surprisingly, most consumers' issues to date with HDMI trace back to HDCP-created root causes.

A scathing article by well-known consumer-electronics-accessories supplier Monster Cable succinctly documented these HDMI woes and their HDCP nexus (**Reference 12**). Common consumer complaints include the inability to get an HDMI-equipped DVD player and display to communicate when an audio/video receiver is between them, for example, whereas the DVD player and display work fine when directly connected. Consumers also complain about the inability to get various pieces of equipment to work unless users power them up in a specific order and the inability to restore previously stable operation once the consumer switches from a particular video source at the display and then switches back.

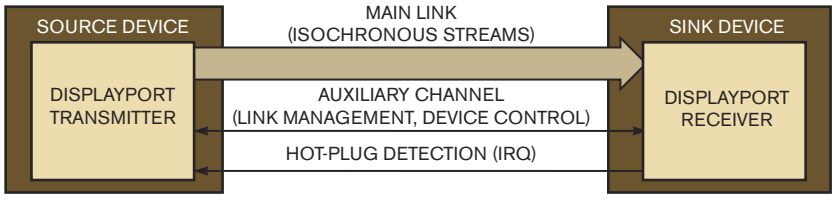

Figure 4 DisplayPort employs packets to transfer audio, video, and other information from source to sink; supplemental buses handle display detection and source and sink interrogation.

The root cause of all these problems is inevitably a disruption in the supposed-to-be-continuous HDCP "handshake" between source and destination, which the video source incorrectly interprets as a DRM breach and responds to by disabling its output. "Ugly" fixes for the problem include power-cycling the equipment or unplugging and replugging connectors to restore normal functions. Even if DRM functions as intended, DVI- and HDMI-equipped video sources often ship factory-configured with their digital outputs inactive, so an owner needs to first connect them to a display over analog connections, reconfigure them in their setup menus, and then reconnect them to the display over a digital link. And, invariably, Monster Cable reports, consumers throw up their hands in dismay and return cabling and gear to the store for refund, a scenario that yields no benefits to the supplier, the retailer, or the end user.

DISPLAYPORT: FALLING SHORT?

The electronics industry has long struggled to discern the differences of, and decide between, the dueling outputs of industry-standards bodies and those of individual companies' or multicompany consortiums' de facto standards. One recent example of this creative tension is the mind-share battle between HDMI and VESA's response: DisplayPort. Although VESA approved DisplayPort specification Version 1.0 in May 2006, I saw a demo of its predecessor, IBM's Digital Packet Video Link, many years earlier at an Intel Developer Forum. As its precursor's name implies, DisplayPort dispenses with the raw video-streaming approach of technologies such as DVI and HDMI, instead bundling audio, video, and control information in packets akin to those found in data networks.

Each DisplayPort Main Link comprises one, two, or four double-terminated differential-signal pairs with no dedicated clock signal; instead, the 8B/10B-encoded data stream embeds the clock (**Figure 4**). AC coupling enables DisplayPort transmitters and receivers to operate on different common-mode voltages and, therefore, to be fabricated on different process lithographies. DisplayPort Version 1.0 specifies both 2.7-Gbps link rates with 270-Mbytes/sec bandwidth per differential-pair lane after subtract-

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Video specs:
- 0.025% differential gain
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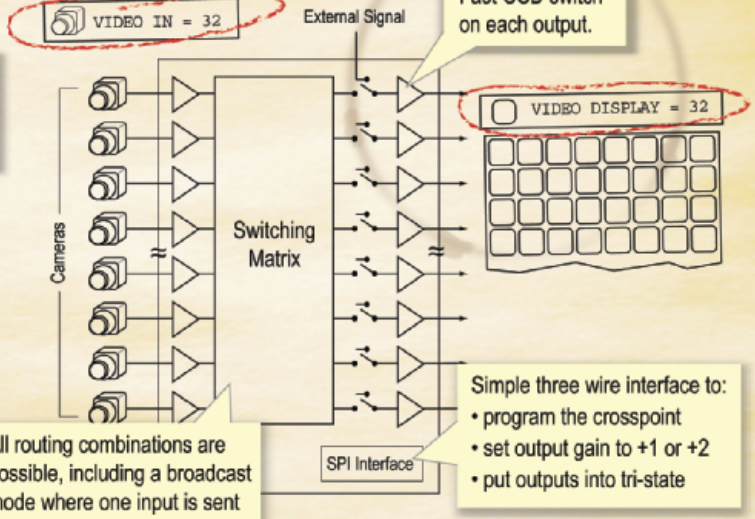
-85dB crosstalk is best among major video switches.

Single-chip 32x32 video crosspoint solution in 356 BGA package.



All routing combinations are possible, including a broadcast mode where one input is sent to all outputs simultaneously.

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ing 8B/10B overhead and 1.62-Gbps link rates with 162-Mbytes/sec bandwidth per lane. The main link is not only high-speed, but also, like HDMI, unidirectional and exhibits claimed, albeit unspecified, low latency. The link rate and pixel rate are decoupled from each other; you can freely trade off pixel depth, resolution, frame rate, and the presence and amount of additional data, such as audio and DRM information in the link stream.

For example, with a one-lane, 2.7-Gbps link, you could alternatively implement a 30-bit/pixel, 4:4:4 YCrCb video stream of 1920×1080-pixel interlaced resolution at 60 fields/sec or an 18-bit/pixel RGB video stream of 1680×1060-pixel progressive-scan resolution at 18-frames/sec. A four-lane DisplayPort link enables you to, for example, implement a 36-bit/pixel 4:4:4 YCrCb video stream of 1920×1080-pixel progressive-scan resolution at 96 frames/sec, a 24-bit/pixel 4:2:2 YCrCb video stream of 1920×1080-pixel progressive-scan resolution at 120 frames/sec, or a 30-bit/pixel RGB video stream of 2560×1536-pixel progressive-scan resolution at 60 frames/sec. Innumerable other combinations are possible for one-, two-, and four-lane main-link configurations, including those that intermingle audio, video, DRM, and other information. A separate half-duplex, bidirectional auxiliary channel with 1-Mbps bandwidth and 500-msec maximum latency handles source/destination handshaking and exchange of source and sink respective capabilities, which a hot-plug-detection interrupt-request signal further supplements.

I attended a detailed technical presentation on DisplayPort at the 2005 SID (Society for Information Display) ADEAC (Americas Display Engineering and Applications Conference) in Portland, OR, when the specification was still in draft form. Both at that event and at a more recent presentation at the SMPTE (Society of Motion Picture and Television Engineers) Technical Conference and Exhibition in Hollywood, CA, I was struck by the fundamental contrast between the technically heavy DisplayPort material and the comparative absence of any tangible industry support. Plenty of companies, many fueled by their distaste for paying DVI and HDMI royalties, are willing to give press-release credence to the DisplayPort approach. But, by press time, Analogix was the only company that had publicly unveiled DisplayPort silicon.

BY PRESS TIME, ANALOGIX WAS THE ONLY COMPANY THAT HAD PUBLICLY UNVEILED DISPLAYPORT SILICON.

DRM until recently also provided a point of differentiation between the dueling display-interface alternatives. Originally, DisplayPort planned to optionally implement Certicom, an obscure DRM technology that Philips developed. HDMI and DVI, in contrast, support HDCP, which has a nearly decade-old implementation history and the all-important backing of heavyweight content-rights holders in Hollywood and elsewhere. Perhaps this fact is the reason that VESA announced in early November 2006 that the upcoming Version 1.1 DisplayPort specification release would add support for HDCP.

FUTURE FORECASTS

A third contender, the Intel-championed UDI (Unified Display Interface), joins DisplayPort and HDMI in the battle to become the next-generation digital interface. The UDI Working Group consortium, also comprising companies such as Silicon Image, Apple Computer, LG, Samsung, and Nvidia, launched itself with fanfare in December 2005, but subsequent progress has been more subdued, even though the Version 1 specification gained approval in July 2006. UDI is a descendant of and backward-compatible with HDMI but delivers as much as 16 Gbps of raw per-link bandwidth. As Wikipedia describes it, "The connector has a single row of 26 contacts pitched 0.6 mm apart from each other, looking very similar to the Intel-initiated USB plug, which has a single row with only four contacts. Three of the 26 contacts will not be wired but are reserved for undetermined future upgrade possibilities. Transmit and receive plugs are slightly different, and a UDI cable will fit only one way. Bidirectional communication works at a much lower data rate than available for the single direction video-data stream" (**Reference 13**). And, at a recent press briefing in San Francisco, HDMI representatives positioned UDI

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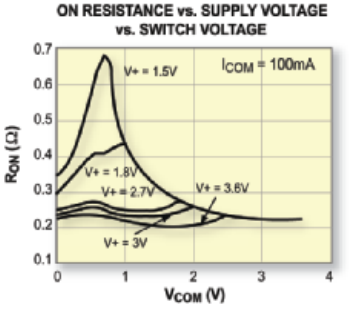
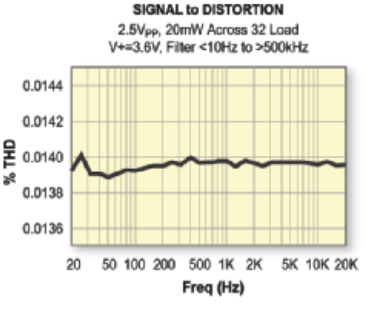
	Device	Function	R_{ON} @ 2.7V (Ω)	R_{ON} Flatness (Ω)	ESD (HBM)	Supply Voltages (V)	Packages
Singles	ISL84714	SPDT/2:1 Mux	0.44	0.06	6kV	1.6 to 3.6	SC70-6
	ISL84715	SPST (NO)	0.26	0.04	4kV	1.6 to 3.6	SC70-5
	ISL84716	SPST (NC)	0.26	0.04	4kV	1.6 to 3.6	SC70-5
	ISL43L210	SPDT/2:1 Mux	0.44	0.06	6kV	1.1 to 4.5	SC70-6
	ISL43L110	SPST (NO)	0.26	0.04	4kV	1.1 to 4.5	SC70-5
	ISL43L111	SPST (NC)	0.26	0.04	4kV	1.1 to 4.5	SC70-5
Duals	ISL84762	2xSPDT/2:1 Mux	0.29	0.03	9kV	1.6 to 3.6	TDFN, MSOP
	ISL84684	2xSPDT/2:1 Mux	0.29	0.03	9kV	1.6 to 3.6	TDFN, MSOP
	ISL8484	2xSPDT/2:1 Mux	0.29	0.03	9kV	1.6 to 4.5	TDFN, MSOP
	ISL43L220	2xSPDT/2:1 Mux	0.23	0.03	9kV	1.1 to 4.5	TDFN
	ISL43L410	DPDT/Diff 2:1 Mux	0.29	0.03	9kV	1.1 to 4.5	TDFN, MSOP
	ISL43L120	SPST (NO)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
	ISL43L121	SPST (NC)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
	ISL43L122	SPST (Mix)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
	ISL43L710	Diff SPST (NO)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
	ISL43L711	Diff SPST (NC)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
	ISL43L712	Diff SPST (Mix)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
Quads	ISL83699	Dual DPDT/Diff 2:1 Mux	0.3	0.06	9/4kV	1.6 to 3.6	QFN, TSSOP
	ISL84780	Dual DPDT/Diff 2:1 Mux	0.45	0.07	4kV	1.6 to 3.6	TQFN, TSSOP
	ISL8499	Dual DPDT/Diff 2:1 Mux	0.3	0.06	9/4kV	1.6 to 4.5	QFN, TSSOP
	ISL43L420	Dual DPDT/Diff 2:1 Mux	0.3	0.06	9/4kV	1.1 to 4.5	QFN
Octals	ISL84781	8:1 Mux	0.41	0.056	4kV	1.6 to 3.6	TQFN, TSSOP
	ISL84782	Diff 4:1 Mux	0.5	0.056	4kV	1.6 to 3.6	TQFN, TSSOP
	ISL43L840	Dual 4:1 Mux	0.5	0.056	4kV	1.6 to 3.6	QFN, TSSOP
	ISL43L841	Diff: 4:1 Mux	0.5	0.056	4kV	1.6 to 4.5	TQFN, TSSOP

ISL84684 Typical Performance





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as a business-class-PC-targeted complementary follow-on to DVI, with greater bandwidth for higher single-link resolution but without HDMI's audio and other enhanced features.

So, what happened to UDI? Intel won't speak on the record about the specification's status, but several anonymous and well-placed industry sources say that Intel has put UDI on the back burner and has shifted its implementation focus to DisplayPort. These sources cite several reasons for the company's change of heart. One is long-standing industry animosity toward HDMI's royalty requirements, which significantly benefited Silicon Image and indirectly also Intel by virtue of its investment relationship. Another reason they cite is a desire to embrace a single standard that could serve both external and integrated graphics subsystem-to-display interconnect schemes, an area in which VESA claimed—and, apparently, Intel agreed—that DisplayPort had an edge over HDMI. Yet another reason could be VESA's belated embrace of HDCP (for which Intel *also* owns fundamental intellectual-property rights).

If the rumors of Intel's still-powerful loyalty switch from HDMI-derived UDI to DisplayPort are true, this change of heart may significantly boost VESA's fortunes. However, you still cannot discount HDMI's notable market lead. HDMI- and DVI-equipped, HDCP-enabled graphics cards are now ramping into production, thereby addressing Windows Vista's DRM requirements (**Reference 14**). HDMI ports are pervasive on HDTVs (high-definition televisions), along with a recently introduced Epson home-theater projector, and are beginning to appear on computer monitors, as well. And HDMI 1.3-equipped consumer-electronics video-source devices, notably Sony's PlayStation 3 and Toshiba's second-generation HD DVD players, are also entering retail channels, based on chips from Silicon Image and other suppliers. Without an immediately obvious technical advantage over HDMI and with slow germination hampering its perception in the market, DisplayPort will be hard-pressed to make any headway at whatever indeterminate point in the future it's ready to do battle. EDN

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DESIGN NOTES

Versatile High Power LED Driver Controller Simplifies Design

Design Note 406

Ryan Huff

Introduction

The increased popularity of high power LEDs over the last several years has challenged electronic engineers to come up with accurate and efficient, yet simple drive solutions. The task is more difficult as the market for LEDs enters the realm of high-powered lights, such as those for automobile headlights or large LCD backlights. High light-output solutions usually involve large arrays of individual LEDs stacked in series. Conventionally, driving high power strings with accurate current is at odds with simplicity and efficiency—typically involving an inefficient linear regulator scheme or a more complicated, multiple IC switching regulator configuration. There is a simpler and better way via a low parts count, single IC solution for driving high power LED strings. At the heart of this highly efficient, simple and accurate solution is the LTC3783 controller IC.

Fully Integrated, High Power LED Driver Controller

The LTC3783 has all of the functions that are normally required to run an LED string: an accurate current regulation error amplifier, a switch mode power supply (SMPS) controller with FET drivers, and two different ways to control the brightness of the LED string.

The current regulating error amplifier uses the voltage drop across a sense resistor in series with the LED string to precisely regulate the LED current. The SMPS control portion of the LTC3783 takes advantage of current mode operation to easily compensate the loop response of the many possible topologies such as boost, buck, buck-boost, flyback and SEPIC. The integrated FET drivers allow fast switching of the power MOSFETs that are needed to efficiently convert input power to LED power without having to add external gate drive ICs.

LED Dimming

Two different ways of controlling LED brightness are included. Analog dimming varies the LED current from a maximum value down to about 10% of this maximum (a 10:1 dimming range). Since an LED color spectrum is related to current, this approach is not appropriate for some applications. However, PWM or digital dimming, switches between zero current and the maximum LED current at a rate fast enough that visual flicker is not apparent, typically greater than 100Hz. The duty cycle changes the effective average current. This method allows up to a 3000:1 dimming range, limited only by the minimum duty cycle. Because the LED current is either maximum or off, this method also has the advantage of avoiding LED color shifts that come with the current changes associated with analog dimming.

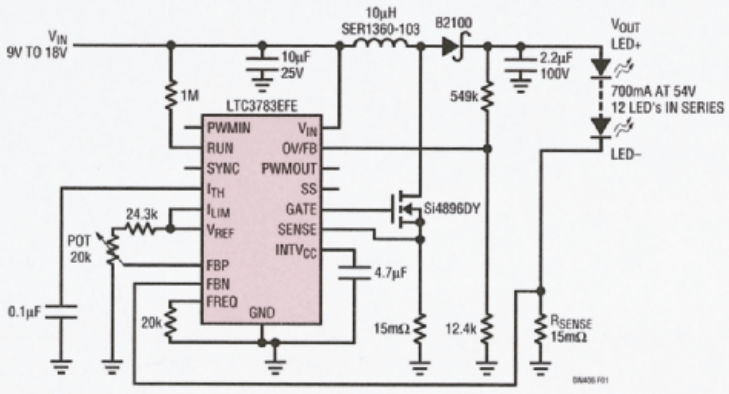

Figure 1. LTC3783 in a Boost Configuration to Drive 12 LEDs in Series

Boost Circuit

Figure 1 shows a boost configuration using all off-the-shelf components. The input voltage, which ranges from 9V to 18V, is boosted to an LED string voltage of 30V to 54V. The LED string can consist of twelve, 700mA LEDs of any color in series for a total of up to 38W of LED power. At an input voltage of 18V and an LED string voltage of 54V, this circuit achieves an astounding power efficiency of over 95%! This high efficiency results in no greater than a 25°C temperature rise for any circuit component.

Buck-Boost Circuit

Figure 2 shows a buck-boost solution that can be used when the input voltage range overlaps the LED string voltage. Here the input voltage ranges from 9V to 36V and the LED string ranges from 18V to 37V. This 8-LED series string runs up to 1.5A. At the nominal input voltage of 14.4V and an LED string voltage of 36V at 1.5A (54W output power), the efficiency is almost 93%. Again, this was achieved using exclusively off-the-shelf components.

LED Protection and Other Features

The LTC3783 can operate from a wide 3V to 36V (or higher) input voltage supply range. A programmable undervoltage lockout ensures that too low of an input voltage is ignored by the chip. If an LED string is inadvertently left open, an overvoltage protection feature ensures that the output voltage does not exceed a programmable level. A soft-start function is included in order to limit the in-rush of current from the input supply during start-up. The switching frequency can be set by a single resistor to any value between 20kHz and 1MHz, or it can be synchronized to an external clock.

Conclusion

Driving high power LED strings with the LTC3783 yields a highly efficient, low parts count and flexible solution. Furthermore, being able to use standard off-the-shelf components helps to simplify the design without sacrificing performance.

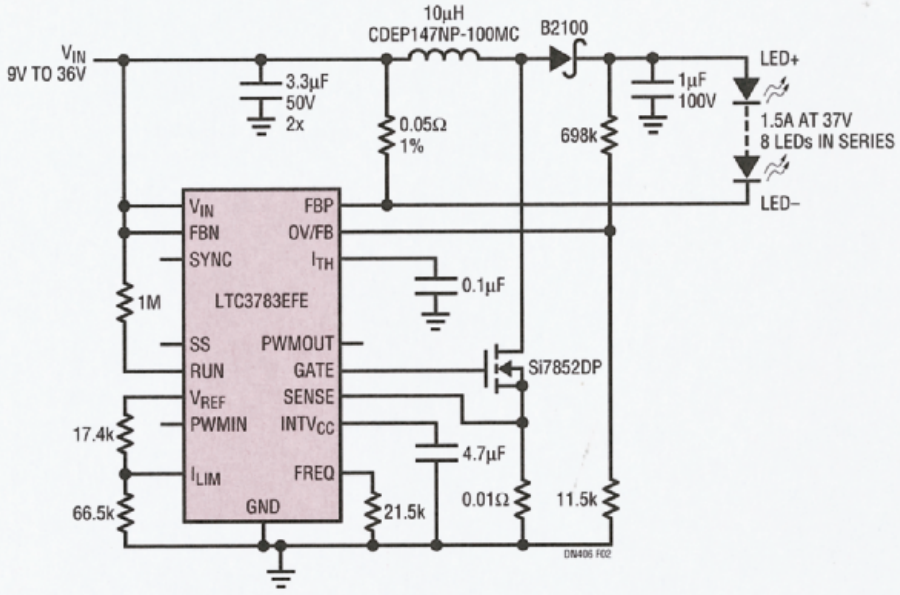

Figure 2. LTC3783 in a Buck-Boost Configuration to Drive 8 LEDs in Series

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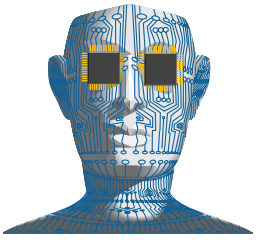

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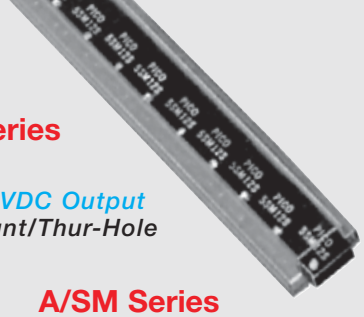

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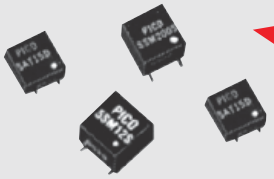

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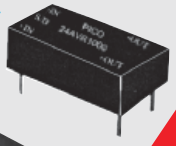

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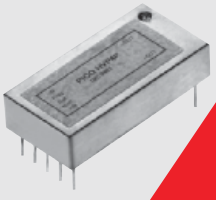

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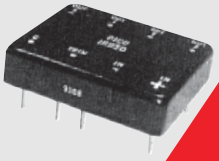

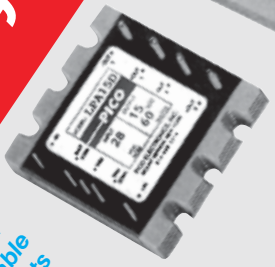

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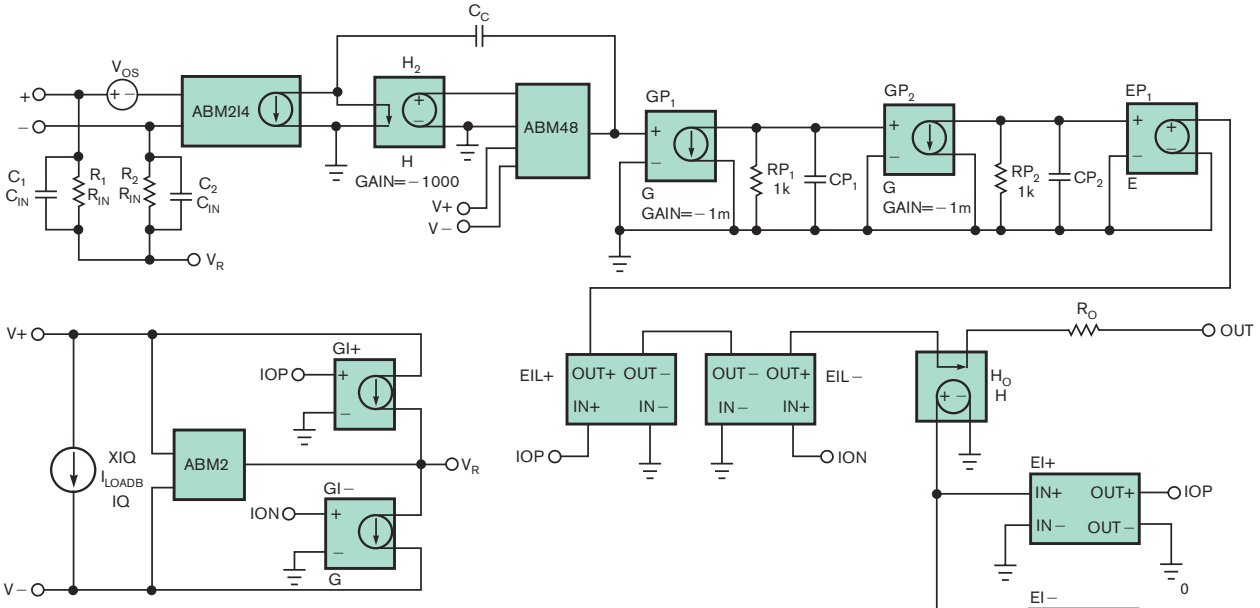
User-friendly model simplifies Spice op-amp simulation

A NEW MACROMODEL BASED ON DATA-SHEET PARAMETERS ALLOWS EASY MODEL CREATION FOR NEW AMPLIFIERS.

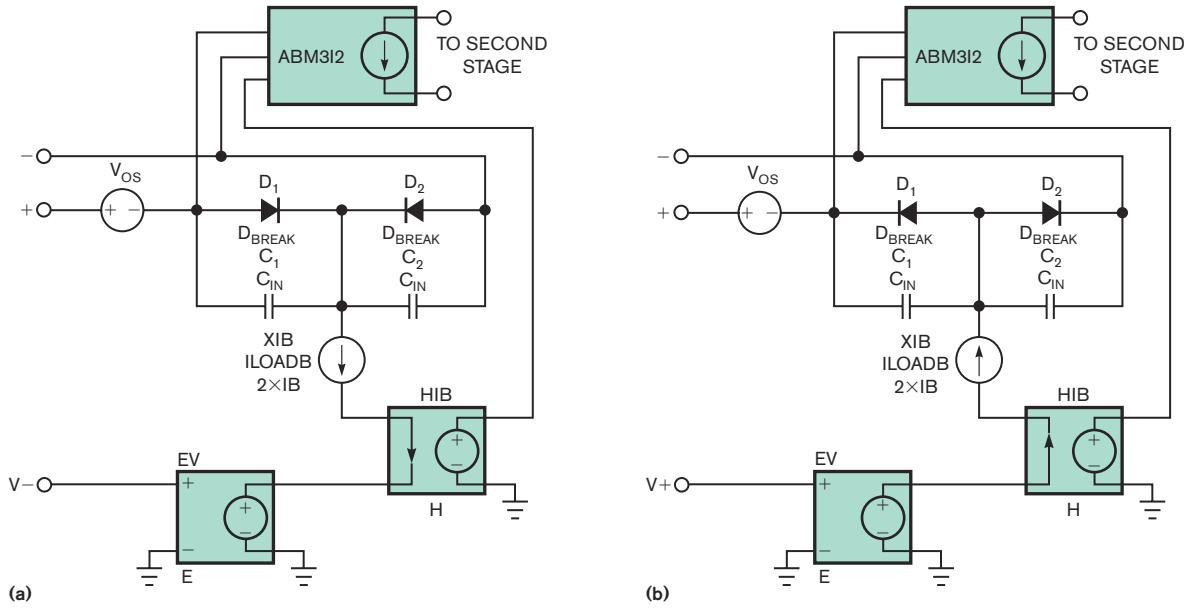
Spice users can run into two types of problems with op-amp models: They need a model that is unavailable in their Spice library, or their library model may produce inaccurate simulation results for their application conditions. This article presents a new op-amp macromodel that makes it easy for any Spice user to create a model for any op amp just by entering parameters from the data sheet. This new macromodel has several advantages over conventional models. It greatly simplifies the creation of new op-amp models, it simplifies the addition of model enhancements and features, and it is more accurate than many other op-amp models.

New op-amp models can be difficult to generate when they aren't in your Spice library or available from an op-amp manufacturer. Many Spice simulators include modeling-utility programs, but they can be difficult to use. Most op-amp models are macromodels that use simplified circuits and functions instead of transistor-for-transistor duplication of the op-amp circuit. Most of the op-amp macromodels in use today are based on a variation of the Boyle model (**Reference**



NOTES:
ABM2I4: LIMIT $((6.28m\times F_U/SR)\times(V(IN_1, IN_2)+(V(IN_1)+V(IN_2))/(2\times CMRR)), -1m, 1m)$.
ABM48: $((V(IN_3, IN_4)-V_{RP}-V_{RN})/3.14)\times ATAN(SR/F_U\times A_V/2\times V(IN_1, IN_2)/(V(IN_3, IN_4)-V_{RP}-V_{RN}))+(V(IN_3)+V(IN_4)-V_{RP}+V_{RN})/2$.
ABM2: $(V(IN_1)+V(IN_2))/2$.
EI+: IF (V(IN+)>0, V(IN+), 0).
EI–: IF (V(IN+)<0, –1×V(IN+), 0).
EIL+: IF (V(IN+)>ILP, 10K×(V(IN+)–ILP), 0).
EIL–: IF (V(IN+)>ILN, 10K×(V(IN+)–ILN), 0).
CP_1 AND CP_2: $1/(6.28K\times F_U\times(128/(90-PM)-0.422))$.
C_C: 1m/SR.

Figure 1 This new op-amp macromodel overcomes many accuracy deficiencies of other models and uses mathematical functions to allow it to use data-sheet parameters for all of its model parameters.



NOTE:
ABM3I2: LIMIT ((6.28m×F_U/SR)×(V(IN_1, IN_2)+(V(IN_1)+V(IN_2))/(2×CMRR)), −1m×V(IN_3)/(2×IB), 1m×V(IN_3)/(2×IB)).

Figure 2 These op-amp model input stages model the input-bias currents of NPN (a) and PNP (b) transistor inputs.

1). Boyle-model parameters bear no easily derivable relation to op-amp-data-sheet parameters, making new models more difficult to generate.

Available op-amp models vary widely in their implementation and can have accuracy limitations that produce incorrect simulation results for some application conditions. For example, many op-amp models incorrectly model the power-supply voltage and current, and some can even produce output voltage with no voltage applied to their power pins. Solutions to many of these problems exist (**Reference 2**, for example), but whether you use an op-amp model from a library or a modeling utility, you can't be sure which electrical characteristics it models accurately without extensive testing.

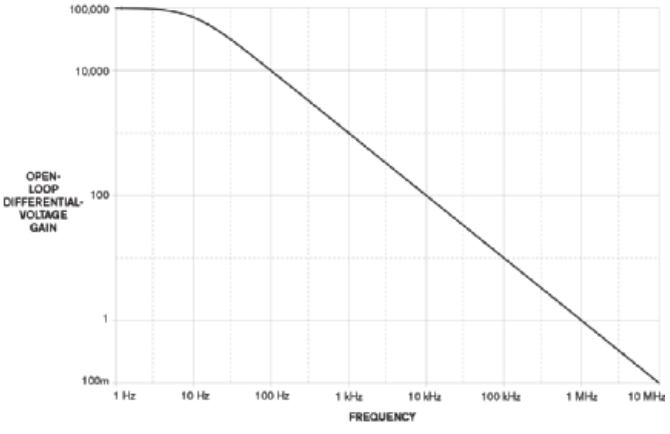


Figure 3 In this plot of open-loop differential voltage gain versus frequency, A_V is 100,000, and F_U is 1 MHz.

A series of articles explains the need for validating op-amp models and some of the tests you can use for verification (**references 3** through **7**).

Figure 1 shows a complete op-amp macromodel that uses mathematical functions instead of the Boyle-model form. This design models the characteristics that most op-amp data sheets define so that the macromodel uses data-sheet parameters for all its model parameters. This feature allows the user to build a new op-amp model just by entering data-sheet parameters. The modular form of the macromodel also makes it much easier for users to add model enhancements and features. This new macromodel overcomes many of the accuracy limitations found in some op-amp-library models. Extensive testing using PSpice demonstrates good convergence and accuracy for a wide variety of simulation types and circuit conditions. This article later describes the remaining limitations.

Figure 1 shows the PSpice macromodel schematic for a high-input-impedance op amp. This general-purpose macromodel works well for FET-input op amps. **Figures 2a** and **2b** show the macromodel-input stages for NPN- and PNP-transistor-input op amps, respectively. **Listing 1**, which is available with the online version of this article at www.edn.com/ms4218, provides corresponding, ready-to-use PSpice-netlist models as subcircuits OPAMPMODH, OPAMPMODN, and OPAMPMODP. You can adapt these macromodels for use with other Spice simulators with analog-behavioral-modeling capability.

The macromodel in **Figure 1**, implemented in model OPAMPMODH, includes stages similar to a real op amp. Mathematical-function block ABM2I4 converts the differential input voltage into a current output as with a typical op-amp-input stage. H_2 functions as an op-amp second stage, converting the current output from the first stage into an amplified voltage. Mathematical-function block ABM48 uses the arc-tangent function to model the op-amp output stage.

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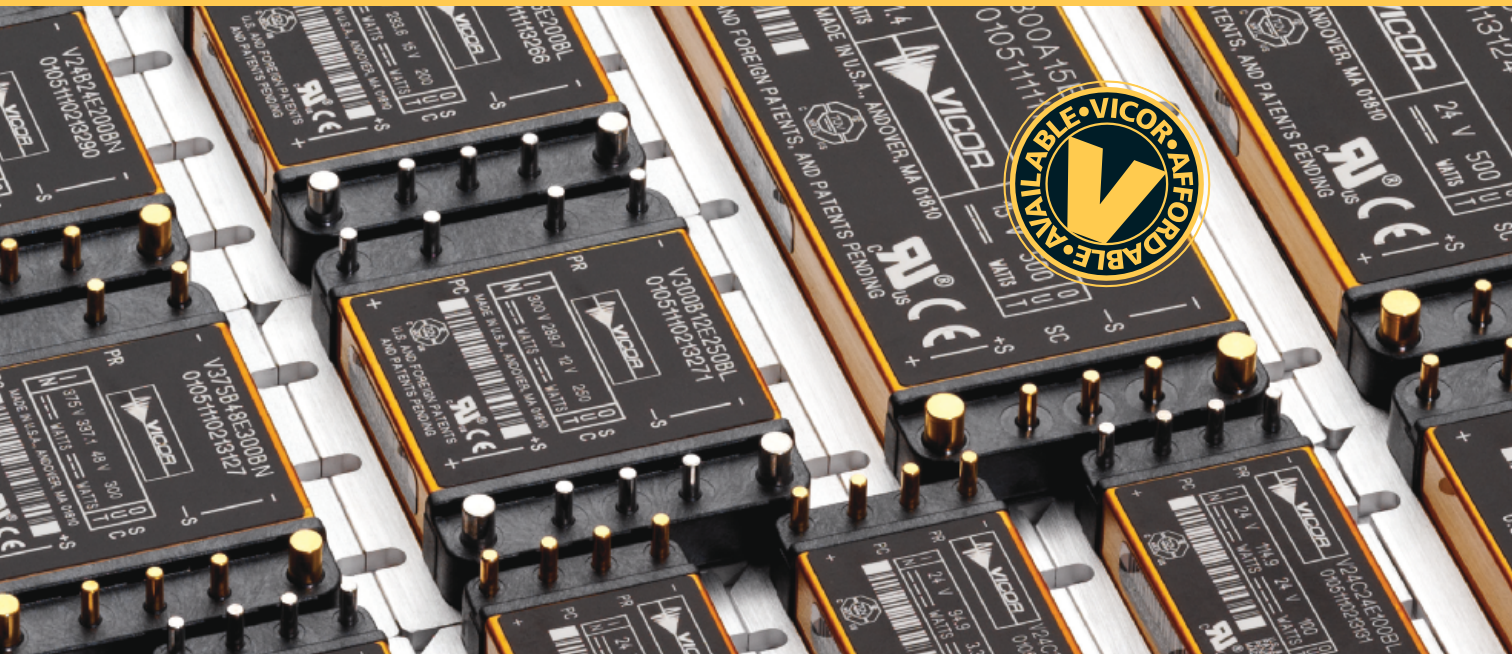

Capacitor C_C models the internal compensation capacitor and the dominant pole of the op amp. These four elements work together to model most of the important characteristics of the op amp (**Reference 8**). The model parameters in the mathematical functions control the macromodel's performance characteristics (see **sidebar** "Macromodel-parameter-selection guidelines" at the Web version of this article at www.edn.com/ms4218). Parameter A_V (open-loop differential-dc-voltage gain) sets the total differential-dc-voltage gain of all the stages. Parameter F_U, the unity-gain frequency, adjusts the small-signal ac characteristics by controlling the transconductance of the input stage. **Figure 3** shows a plot of the macromodel-frequency characteristics with an A_V of 100,000 and an F_U of 1 MHz. Parameter SR (slew rate) models the maximum slew rate using the limit function to control the maximum charge rate of capacitor C_C. **Figure 4** shows a plot of the macromodel-voltage-follower pulse response with a slew rate of 1 MV/sec. Parameter CMRR (common-mode-rejection ratio) sets the dc common-mode gain relative to the differential gain. The macromodel produces the same relative ac characteristics for the differential- and the common-mode response. Parameters V_{RP} (positive-rail voltage) and V_{RN} (negative-rail voltage) control the output-voltage-swing limits. **Figure 5** shows a plot of the macromodel's dc response to differential input with an A_V of 100,000, a V_{RP} and a V_{RN} of 1V, and power of ±15V.

The simplest method of modeling op-amp stability uses the phase margin, a measure of how close the op amp is to oscillating at the unity-gain frequency. The phase margin depends on the high-frequency, nondominant poles of the op amp. The macromodel uses GP_1, GP_2, EP_1, RP_1, RP_2, CP_1, and CP_2 to generate two identical high-frequency poles, resulting in an overall output-phase shift of 180° at the pole frequency. The capacitance values of CP_1 and CP_2 use equations to relate the PM (phase-margin) parameter to this pole frequency. **Figure 6** shows a plot of the macromodel phase response with an F_U of 1 MHz and a PM of 30°, producing a phase shift of 150°—that is, 180° minus PM—at an F_U of 1 MHz. You can also adjust PM so that the macromodel matches the op-amp pulse-response overshoot.

The quiescent current of most op amps is relatively independent of supply voltage. XIQ (subcircuit ILOADB in **Listing 1**) determines the macromodel's quiescent power-supply current. ILOADB uses the Spice JFET model to produce a constant-current load but only if a voltage is present. The parameter IQ determines the value of the current. Voltage source ABM2 generates V_R as a reference voltage halfway between the power-supply-voltage inputs. The macromodel uses V_R instead of ground as a reference for the input signals. Note that the currents into and out of node V_R do not affect its voltage level.

Several macromodel functions depend on the output current. Current-controlled voltage source HO measures the macromodel output current, which EI+ and EI− use to generate the IOP and ION functions. IOP corresponds to the positive (source) current of the macromodel, and ION corresponds to the negative (sink) current. GI+ and GI− use IOP and ION, respectively, to draw additional load current from the power-supply-voltage inputs, correctly modeling the

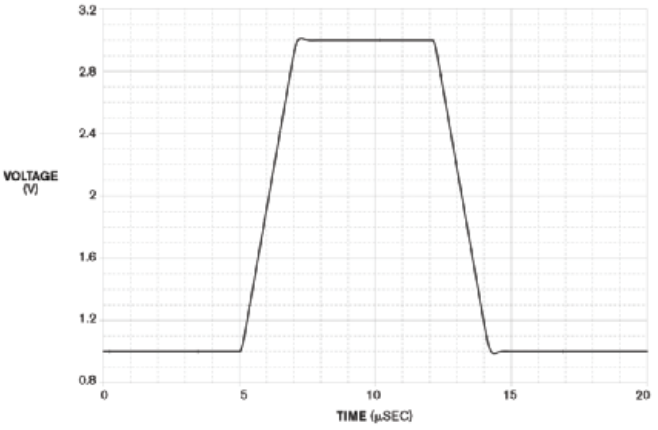

Figure 4 In this plot of the macromodel-voltage-follower pulse response, the slew rate is 1 MV/sec.

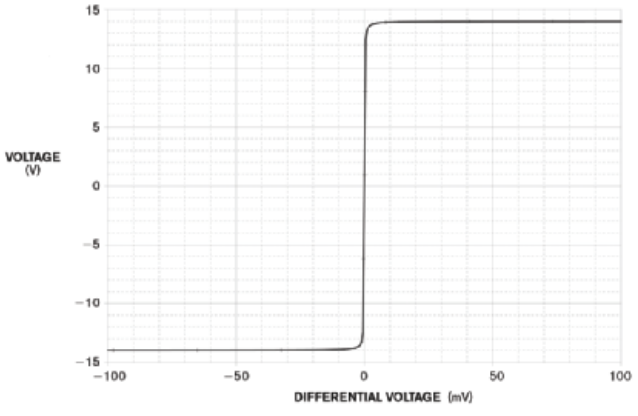

Figure 5 In this plot of the macromodel's dc response to differential input, A_V is 100,000, V_{RP} and V_{RN} are 1V, and power is ±15V.

splitting of output current between the power-supply rails. **Figure 7** shows a plot of the macromodel's output current and supply currents with IQ of 0.5 mA.

The output stage of an op amp can produce only a limited amount of output current. This current limit is often different for positive (source) and negative (sink) output currents. To model these current limits, EIL+ and EIL− limit the positive and negative output current of the macromodel to the values set by parameters ILP and ILN, respectively. EIL+ and EIL− have no effect on the output voltage unless the output current begins to exceed ILP or ILN. When that situation occurs, either EIL+ or EIL−, depending on the polarity of the current, reduces the magnitude of the output voltage to regulate the output current to the value of ILP or ILN.

Resistor and parameter R_O set the macromodel's output resistance. Voltage source and parameter V_{OS} set the input

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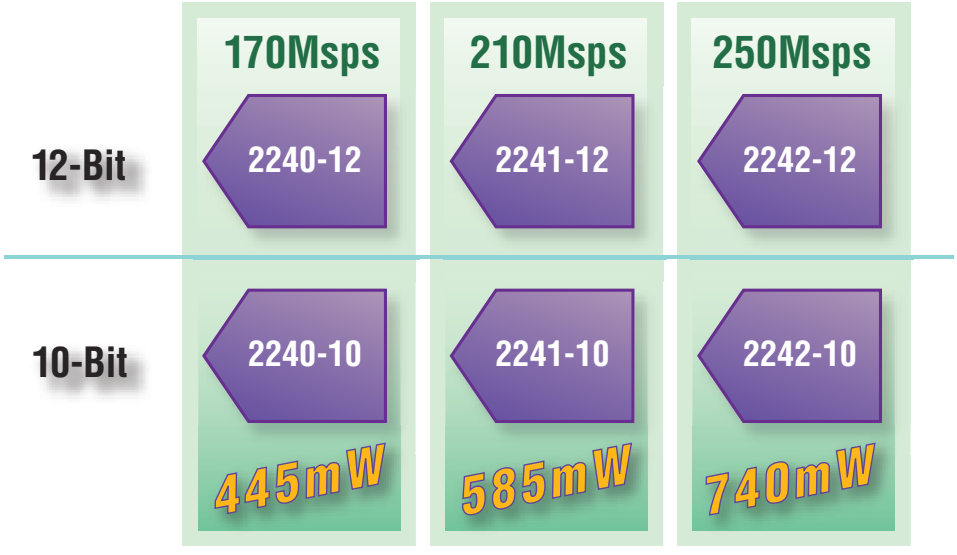

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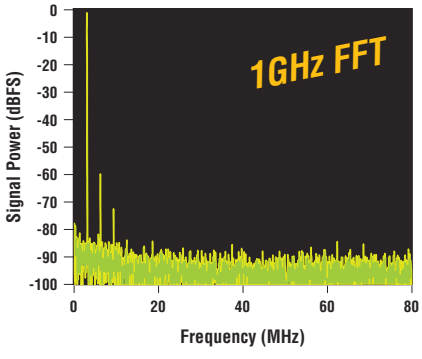

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offset voltage. R_1, R_2, C_1, and C_2, along with parameters R_{IN} and C_{IN}, set the input resistance and capacitance. The simple input resistance model in **Figure 1** provides a good approximation for high-impedance op amps, especially FET-input op amps, but it does a poor job of modeling the input bias currents of NPN and PNP transistor inputs. The macromodel input stage in **Figure 2a**, implemented in model OPAMPMODN, solves this problem by using diodes D_1 and D_2 to model the base-emitter junctions of the NPN input transistors. XIB uses subcircuit ILOADB and parameter I_B to model the input bias current entering the op-amp inputs for NPN transistors. When the inputs are below the functional range of the op amp and both of the input junctions are reverse-biased, the input bias current drops to zero, turning off the op amp. The macromodel models this characteristic using ABM3I2 for the input stage so it can sense the input bias current using HIB. When the bias current drops to zero, ABM3I2 uses the limit function to reduce its output current to zero. The macromodel-input stage in **Figure 2b**, implemented in model OPAMPMODP, models the corresponding input stage for PNP-transistor inputs, with the input bias current leaving the op-amp inputs.

MACROMODEL LIMITATIONS

All simulation models have some accuracy limitations, and this new op-amp macromodel is no exception. Though the macromodel's limitations do not cause problems for most circuit conditions, it is important to remain aware of these limitations so that you can avoid applications that produce erroneous analysis results. Op amps generally have several high-frequency poles and, often, zeros that affect the stability and phase margin, instead of the two high-frequency poles that the macromodel uses. Only the part manufacturer typically knows where the high-frequency poles and zeros are, and data sheets typically do not provide this information. In some cases, you could achieve better model accuracy for stability and overshoot by modeling all the high-frequency poles and zeros. If this level of accuracy is necessary and if you know where the high-frequency poles and zeros are, you can add pole and zero stages to the macromodel using well-documented techniques (**Reference 9**).

Op amps can operate properly only within a limited range of input voltages. This range generally includes a portion of the voltage between the power-supply rails. The NPN- and PNP-input macromodels do a good job of modeling the portion of the input-voltage range for which the input junctions are reverse-biased. The high-input-impedance macromodel places no limits on the input voltages for proper operation, unlike a real op amp.

The macromodel does not include the ability to model output variations with changes in power-supply voltage (power-supply-rejection ratio). The Arctangent function for modeling the output stage does not lend itself to modeling this characteristic. The current version of the macromodel also lacks features for modeling variations in performance characteristics with temperature and modeling of ac noise. The modular form of the macromodel lets you add these features if necessary. EDN

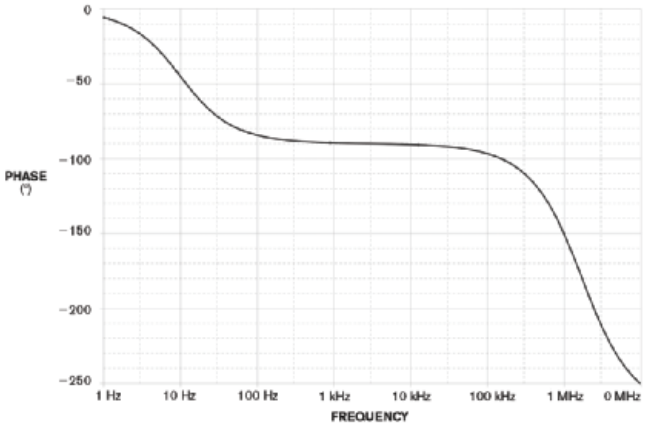

Figure 6 In this plot of the macromodel phase response, F_U is 1 MHz and PM is 30°, producing a phase shift of 150°—that is, 180° minus PM—at an F_U of 1 MHz.

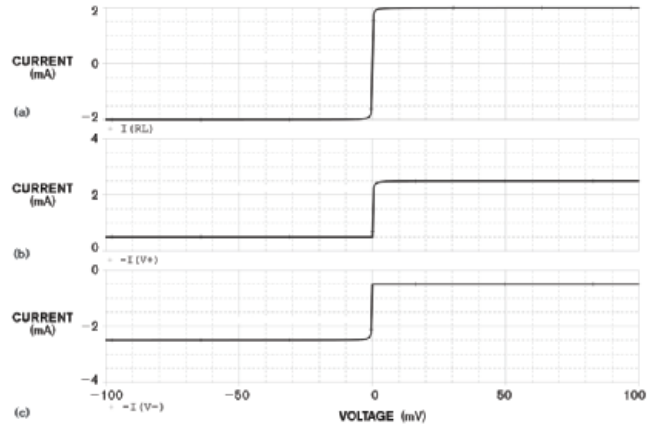

Figure 7 In this plot of the macromodel's output current (a), positive-supply current (b), and negative-supply current (c), IQ is 0.5 mA.

REFERENCES

For the complete list of references for this article, go to www.edn.com/ms4218.

AUTHOR'S BIOGRAPHY

Ray Kendall is a principal engineer at Intuitive Research and Technology Corp (Huntsville, AL, www.irtc-hq.com), where he designs, analyzes, and integrates high-reliability electronic circuits and systems, including numerous defense and NASA systems. He specializes in circuit simulation and modeling using PSpice. He is a licensed professional engineer and holds a bachelor's degree in electrical engineering from the University of Mississippi (University) and a master's degree in engineering from the University of Alabama—Huntsville.

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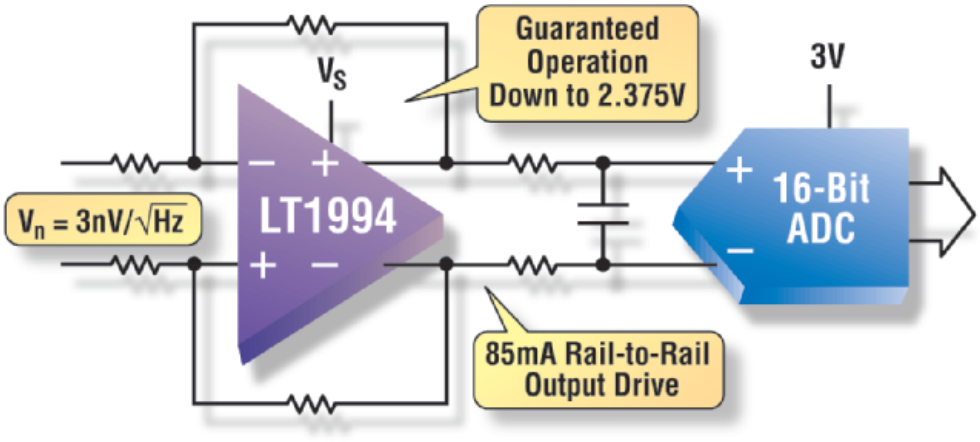

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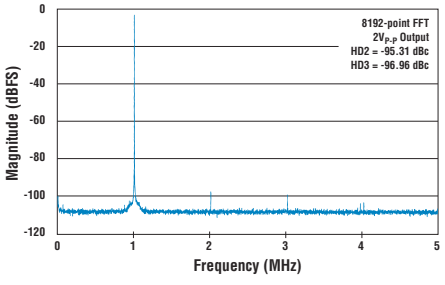

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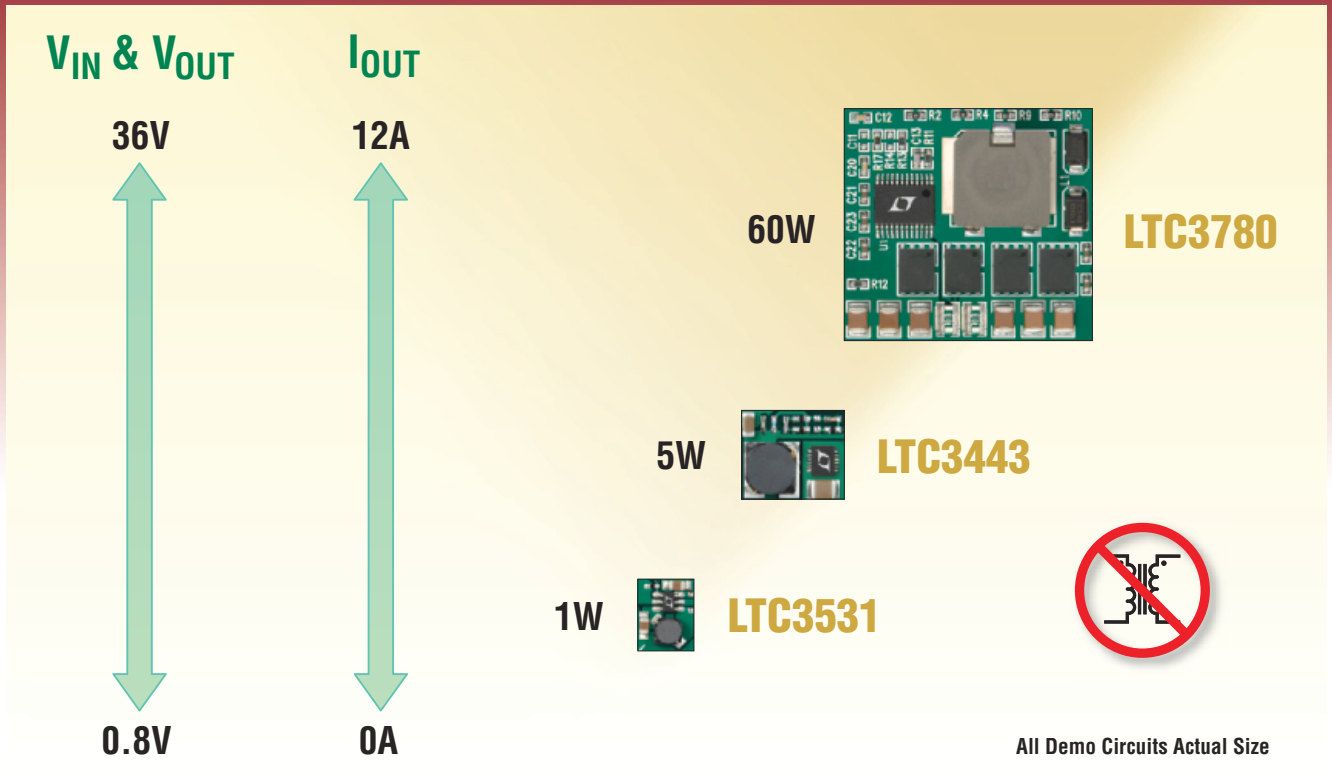

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LTC3440	2.5 to 5.5	2.5 to 5.5	0.6	300kHz to 2MHz	25	3x3 DFN, MSOP-10
LTC3530	1.8 to 5.5	1.8 to 5.25	0.6	300kHz to 2MHz	40	3x3 DFN, MSOP-10
LTC3441	2.4 to 5.5	2.4 to 5.25	1.2	1MHz	25	3x4 DFN
LTC3442	2.4 to 5.5	2.4 to 5.25	1.2	300kHz to 2MHz	35	3x4 DFN
LTC3443	2.4 to 5.5	2.4 to 5.25	1.2	600kHz	28	3x4 DFN
LTC3785*	2.7 to 10	2.7 to 10	10.0†	100kHz to 1MHz	80	4x4 QFN, SSOP-28
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† Depends on MOSFET selection, *Future Product

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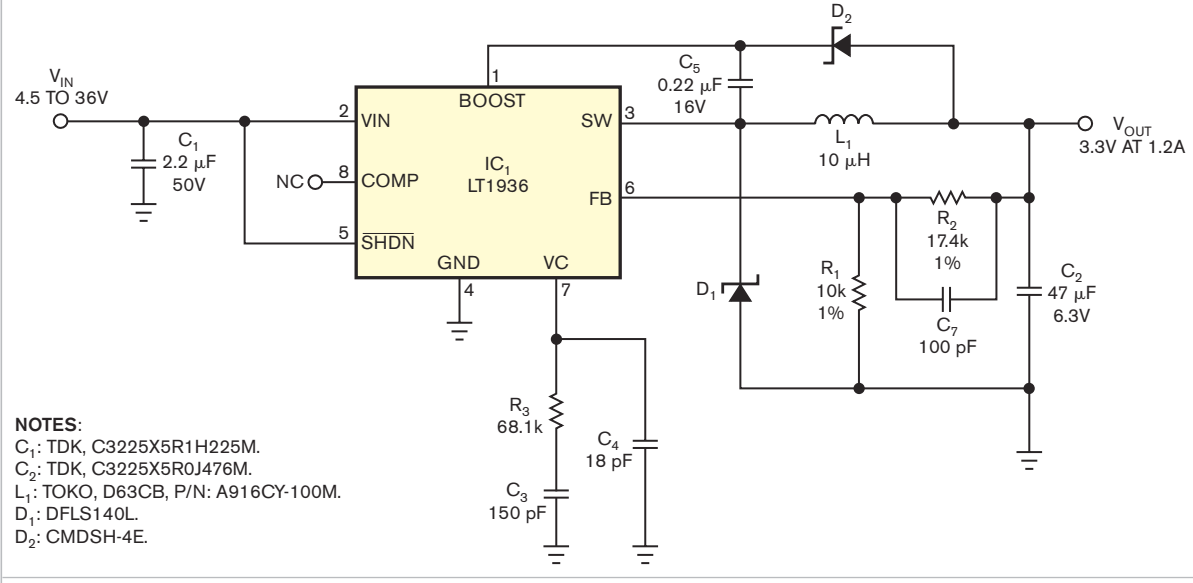
Extend low-output-voltage switching regulator's input range

Hua (Walker) Bai, Linear Technology, Milpitas, CA

Internal operating voltages in electronic devices continue to decrease, but input-source voltages don't change. As the difference between input and output voltages increases, so does the improvement in efficiency that a switching regulator offers. Unfortunately, as a switched-mode step-down converter's output voltage decreases, the decrease imposes limitations on the circuit's input-voltage range. This Design Idea shows how to extend a low-output-voltage step-down converter's input-voltage range.

A switching-mode step-down regulator, such as Linear Technology's (www.linear.com) LT1936 (IC_1), includes an internal high-side NPN power transistor between its input, V_{IN}, and switched-output (SW) pin. For highest efficiency, the high-side NPN transistor requires a base voltage that's higher than the input voltage. The circuit of **Figure 1** works best for output voltages greater than 3V. A charge pump comprising diode D_2 and capacitor C_5 maintains the voltage at the Boost pin 3V above V_{IN}. When IC_1's internal power transistor switches off, the voltage at SW goes to ground through D_1. Boost capacitor C_5 charges to 3V supplied from V_{OUT} through D_2. When the power transistor turns on, the voltage at SW jumps to V_{IN}, and the voltage at the Boost pin jumps to $V_{IN}+3V$, which provides sufficient head room to drive the power transistor into saturation for greatest efficiency.

However, output voltages below 2.8V no longer provide sufficient drive volt-



NOTES:
C_1: TDK, C3225X5R1H225M.
C_2: TDK, C3225X5R0J476M.
L_1: TOKO, D63CB, P/N: A916CY-100M.
D_1: DFLS140L.
D_2: CMDSH-4E.

Figure 1 For efficient operation at output voltages of 3.3V or higher, a charge pump comprising D_2 and C_5 provides a voltage boost that provides sufficient drive for IC_1's internal switching transistor.

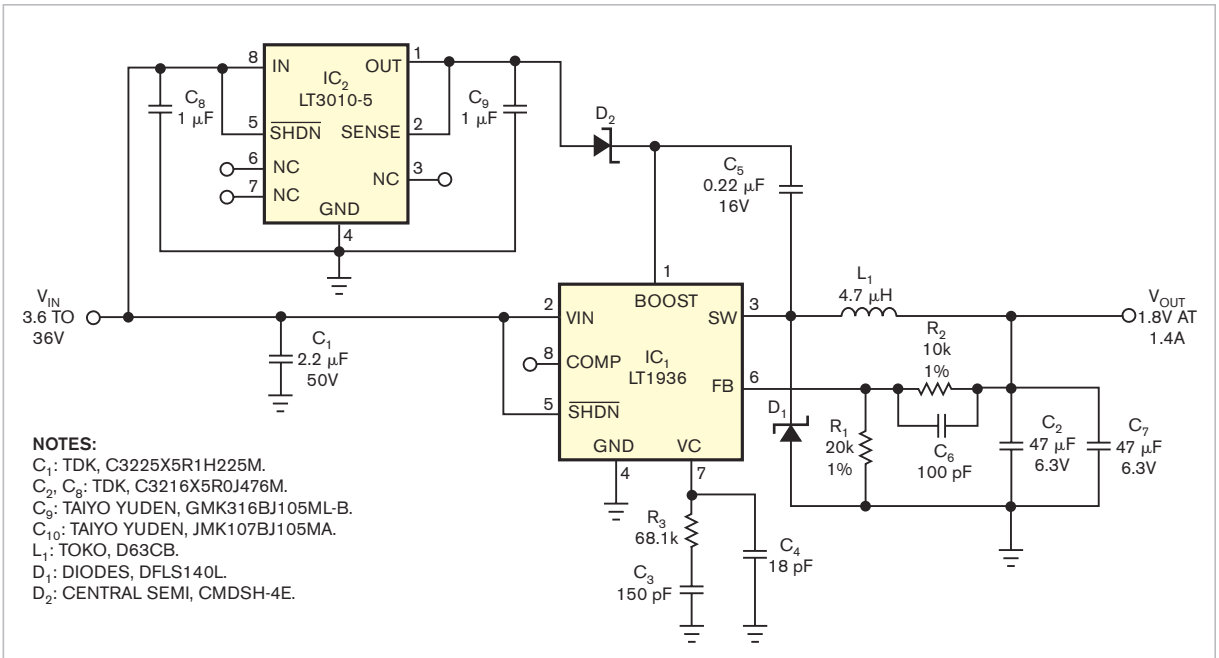


Figure 2 At outputs as low as 1.8V, efficient operation at low input voltages benefits from an added low-dropout regulator, IC_2, for the Boost pin, which extends the circuit's input-voltage range.

age to fully saturate IC_1's switching transistor, and the circuit's efficiency suffers due to increased voltage drop across the transistor. In this situation, connecting D_2's anode to V_{IN} instead of V_{OUT} doubles the Boost pin's voltage to twice the value of V_{IN} but limits V_{IN} to 20V to avoid exceeding the Boost pin's allowable maximum voltage. For outputs lower than 2.8V, the circuit in **Figure 2** extends V_{IN}'s maximum voltage to 36V. When the input exceeds 5.3V, a Linear Technology LT3010-5 low-dropout voltage regulator maintains the voltage across C_9 at 5V. As a result, for input voltages at V_{IN} of 5.3 to 36V, the voltage at the Boost pin always remains at 5V above V_{IN}. **Figure 3** shows a 36V input applied to V_{IN} and the resultant voltages at the SW and Boost pins. In **Figure 3**, the maximum Boost-pin voltage reaches 41V, safely below the pin's 43V maximum rating. For values of V_{IN} of 3.6 to 5.3V, IC_2 operates in dropout mode and introduces only a 300-mV drop from its input to its output. **Figure 4** shows that, even at the circuit's minimum 3.6V input, the Boost pin remains 3.3V above V_{IN}, and IC_1's internal NPN transistor receives sufficient drive voltage for saturated operation. EDN

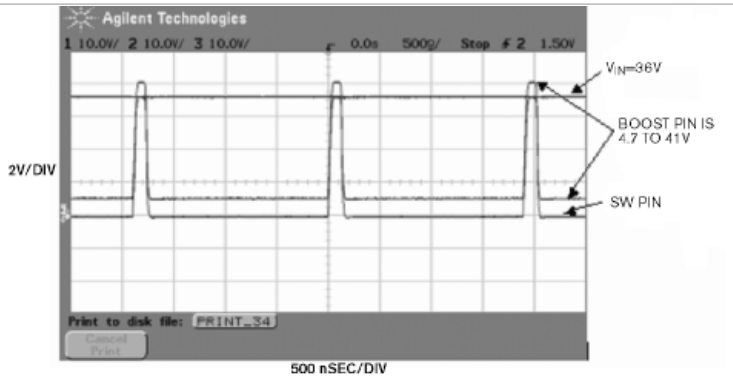


Figure 3 At a maximum input voltage of 36V (V_{IN}), waveforms at the SW and Boost pins show a 5V boost-voltage margin for the circuit of Figure 2.

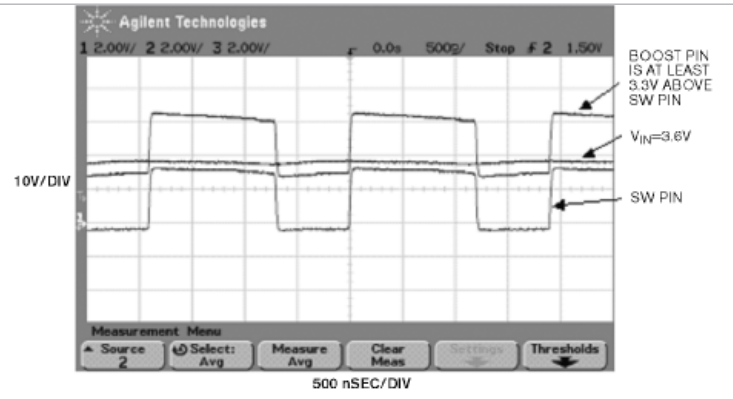


Figure 4 At 3.6V input (V_{IN}) and 1.8V output, a voltage of 3.3V at IC_1's boost pin ensures that IC_1's internal switch still operates in saturated mode.

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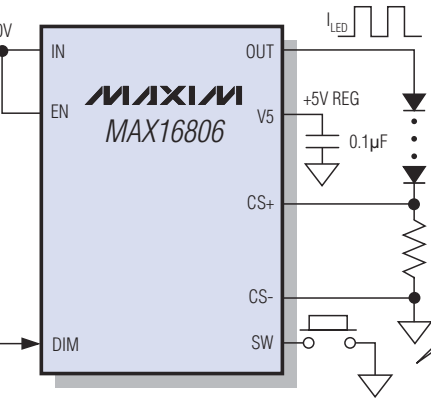

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MAX16803	✓	✓	✓	✓	✓					
MAX16804	✓	✓	✓	✓	✓	✓				
MAX16805	✓	✓	✓	✓	✓	✓	✓	✓		
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Automatic latch-off circuit saves batteries

Kieran O'Malley, On Semiconductor, West Kingston, RI

Although rechargeable batteries offer many advantages, they can suffer damage and shortened service lives if they're fully drained of their charge. The circuit in **Figure 1** shuts off a battery-powered appliance—in this instance, an LED flashlight receiving power from NiMH (nickel-metal-hydride) cells—when the battery voltage falls below a preset limit. Although intended for an LED flashlight, this circuit can apply to any battery-powered application. Without ensuring that the user will remove the batteries for recharging, this circuit latches the flashlight off when the battery voltage falls below the usable limit and thus provides a strong hint that it may be time to recharge.

Although a simple nonlatching voltage comparator can switch off power, removing the battery's load causes a voltage rebound, and the comparator restores power, forcing the light into a flashing mode. This circuit turns off the flashlight, and it remains off until the user manually turns on the light using switch S_1.

A 600-mA NCP1421 PFM step-up synchronous-rectifier dc/dc-converter, IC_1, from On Semiconductor (www.onsemi.com) forms the heart of the circuit, but the basic design applies to many other converters offering similar features (**Reference 1**). The NCP1421's key features include an integrated LBI/EN (low-battery input/enable) and an open-drain LBO (low-battery output). Operating from two AA-size NiMH batteries, the circuit comprises the components of a normal boost regulator: an inductor, input and output capacitors, and a current-sense circuit to the right of IC_1. A combination of the LED's forward voltage, which R_3 and R_2 divide down, and voltage across current-sense resistor R_1 produces a feedback voltage for comparison with the NCP1421's 1.2V nominal reference voltage.

On the input side, IC_1's LBI/EN pin connects to the battery through a voltage-divider network formed by resistors R_4, R_5, and R_{10}. The NCP1421 remains enabled while the voltage on LBI/EN exceeds 1.2V. When the voltage on LBI/EN falls below 1.2V, the LBO-detector pin goes low, switching on Q_3 and supplying current to Q_1's base. When Q_1 switches on, Q_2's base goes low and latches the virtual SCR (silicon-controlled rectifier) formed by Q_1 and Q_2, an MBT3946DW1 integrated dual transistor, IC_2.

In addition, Q_1 latches the LBI/EN pin low to prevent IC_1 from turning on again upon load removal. To restart the circuit, switch S_1 must interrupt the circuit's power. Resistors R_4, R_5, and R_{10} set the battery-voltage trip point for the LBO detector. R_5 also sets the current drawn from the battery when the SCR activates. The circuit switches off when the battery voltage drops to approximately 1.3V, a point at which the LBI/EN pin reaches 1.2V. EDN

REFERENCE

1 NCP1421 data sheet, www.onsemi.com/pub/Collateral/NCP1421-D.PDF.

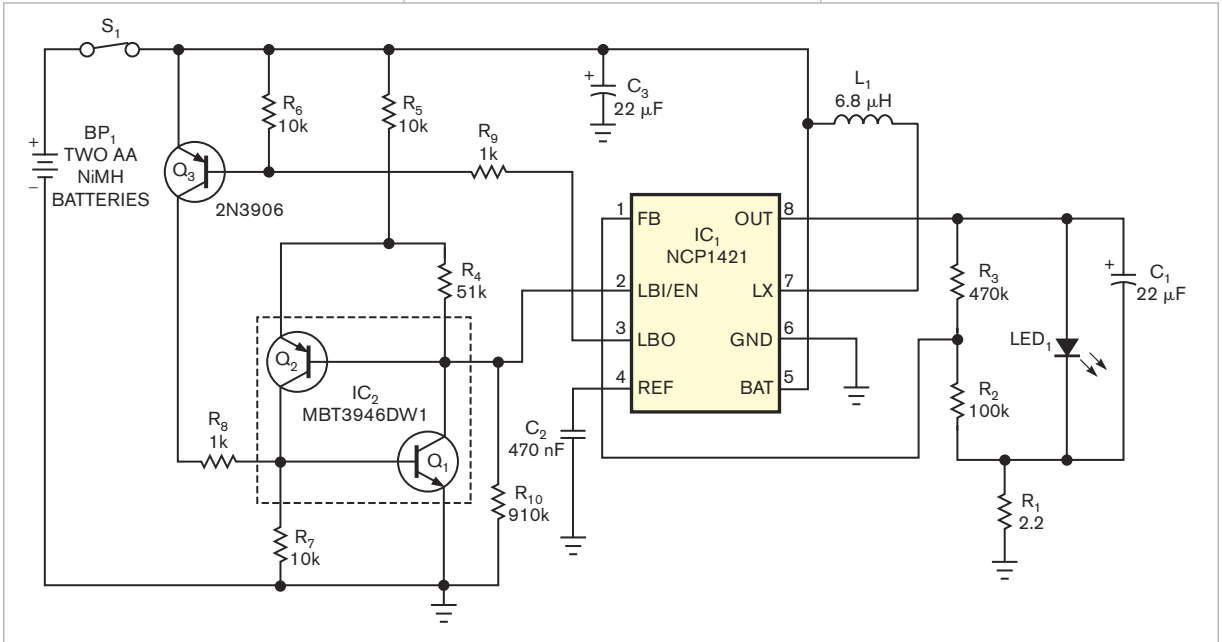

Figure 1 This circuit extends the lives of rechargeable batteries by removing power at a preset voltage and preventing overdischarge.

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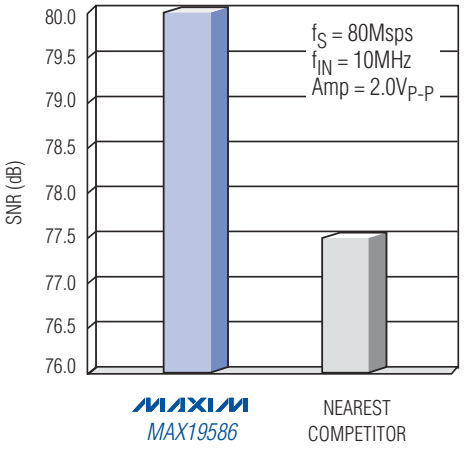

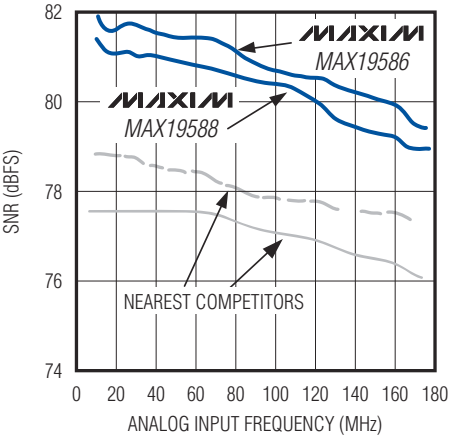

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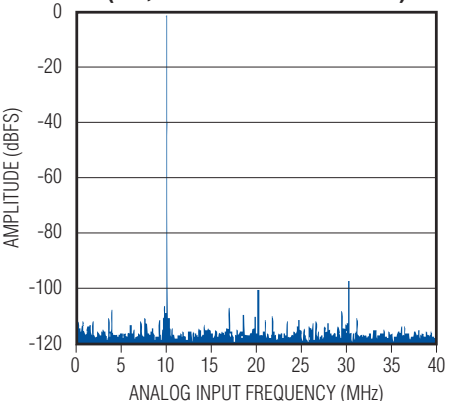

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Switching regulator reduces motor brake's power consumption

Alain Minoz, Elekta Instrument AB, Stockholm, Sweden

For safety reasons, a motor that drives a safety-critical electromechanical assembly often includes an electromagnetic brake on its drive shaft. The brake typically comprises a solenoid coil that actuates a mechanical clutch, and, when you power it, the brake allows the drive shaft to rotate. Although simple and robust, the brake requires a lot of energy to release the clutch and then much less energy to remain actuated.

Measurements show that a brake rated for 24V dc requires a minimum of 18V to release and as little as 8V holding voltage. Substituting those numbers into the equation $P_{COIL}=V^2/R_{COIL}$ shows that, while actuated, the brake consumes less than a quarter of the power required for its initial release. Conversion of excess release power into heat normally doesn't pose problems. However, a precision positioner that uses a brake mounted on a long drive screw can suffer from unacceptable errors if the heat expands the drive screw and alters the assembly's position.

One method of solving the problem involves actuating the brake by applying 24V dc for a brief interval and then reducing the holding voltage to 12V. Under these conditions, the brake dissipates only a quarter of the initial power and thus operates at a reasonable temperature. **Figure 1** shows the influence of actuation voltage on the brake's temperature. As expected, lowering the voltage after actuation drastically lowers the brake's temperature and therefore its effects on the positioning screw.

Figure 2 shows one obvious voltage-reduction approach, which uses relays and a power resistor to halve the voltage applied to the brake. Setting the current-limiting resistance, R_{POWER}, equal to the brake's solenoid resistance, R_{BRAKE}, reveals a few problems. First, the power resistor must dissipate as much power as the brake solenoid's coil. Second, the relays and power resistor occupy considerable space on a pc board. Third, proportioning the values of the R_1C_1 delay circuit's components to achieve a few seconds' delay can prove difficult.

Figure 3 shows another approach, which uses the actuator coil's inductance and replaces relays with an IC. The voltage you apply to the brake need not be continuous, and applying a PWM (pulse-width-modulated) voltage works as well as applying a dc holding voltage because the coil's inductance integrates the current pulses.

A switched-mode voltage regulator can provide an inexpensive and effective PWM-drive voltage. For example, National Semiconductor's (www.national.com) LM2575 adjustable regulator, IC_1, operates over a 7 to 40V range and includes an on/off-control input and a high-impedance feedback input, but any other switching-regulator IC with these two characteristics would also serve. Resistors R_1 and R_2 determine the holding voltage (**Figure 4**). Capacitor C_3 filters the PWM signal to a dc voltage at the feedback input and also maintains the feedback input for a few seconds during start-up at ground, forcing the regulator to deliver the full input voltage to actuate the brake. Diode D_1 quickly discharges the capacitor when the regulator switches off, diode D_2 clamps the switch-off transient voltage that the brake's actuating coil produces, and diode D_3 protects IC_1 against reverse voltage. Photocoupler IC_2 isolates the brake controller from the control circuit.

During start-up, the duration of the regulator's 24V actuation-pulse output fluctuates from 1 to 4 seconds (**Figure 4**). Fortunately, the variation has no impact on the circuit's function but could

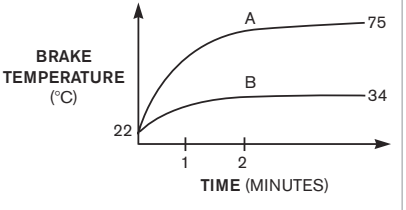

Figure 1 Under continuous operation with 24V applied, the brake's temperature stabilizes at 75°C, or 53°C above ambient temperature (Curve A). Applying a 24V actuation pulse for a few seconds and then applying a 12V holding voltage stabilizes the brake at 34°C, or only 12°C above ambient temperature (Curve B).

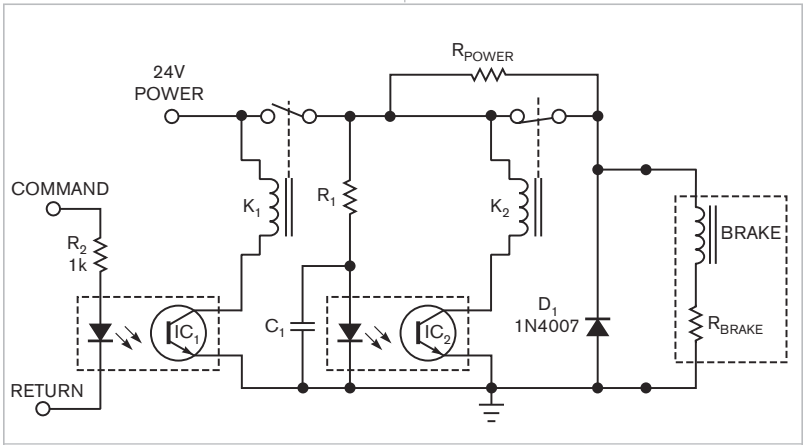

Figure 2 Actuating the brake release trips relay K_1 and applies 24V to the brake. An RC network delays K_2's actuation. When normally closed relay K_2 opens, resistor R_{POWER} reduces the voltage applied to the brake to the holding level.

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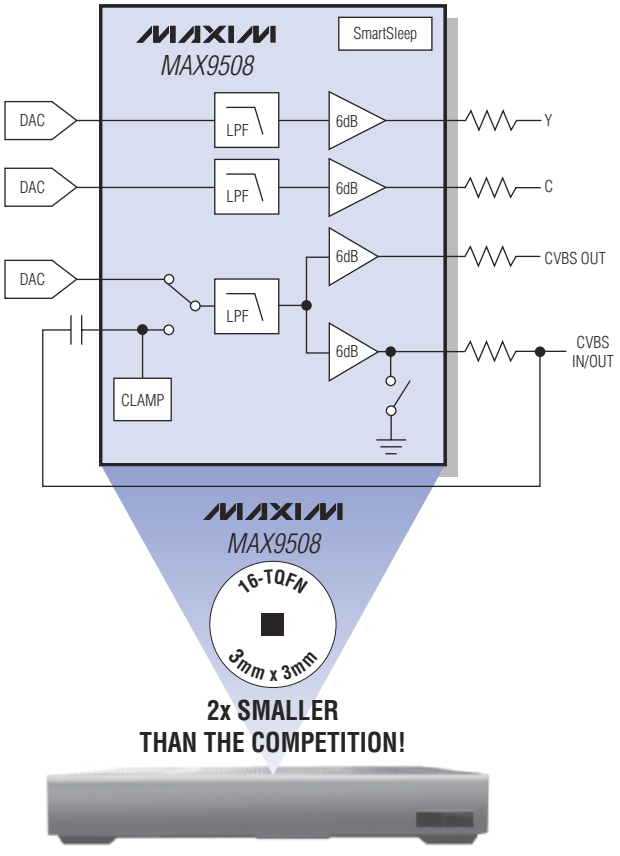

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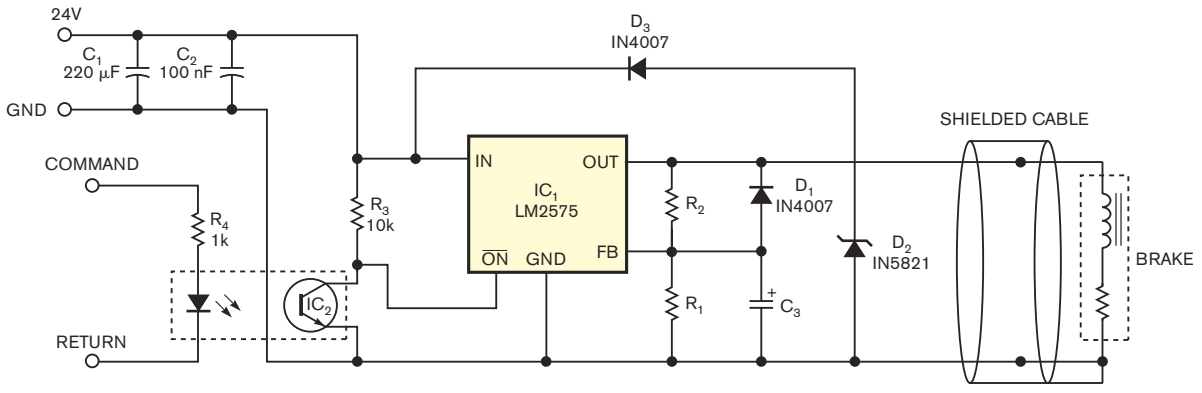

Figure 3 Applying the command input switches on PWM regulator IC_1, and capacitor C_1 holds IC_1's feedback input low, applying a maximum output voltage of 24V to the brake until C_1 fully charges. As the feedback voltage slowly rises to 1.23V, the regulator's output voltage decreases to approximately 12V, the brake's nominal holding voltage.

present a problem if another application requires a precisely timed actuation pulse. After start-up, the regulator delivers a 12V holding voltage, reducing the power demand to one-quarter of the start-up value. As a bonus, the circuit uses inexpensive components, occupies only a few square centimeters of pc-board area, and eliminates the need for two electromechanical relays. Wiring for the PWM-drive voltage can radiate electrical noise unless the circuit is adjacent to the brake. For remote installation, use a shielded twisted-pair cable to minimize noise radiation. EDN

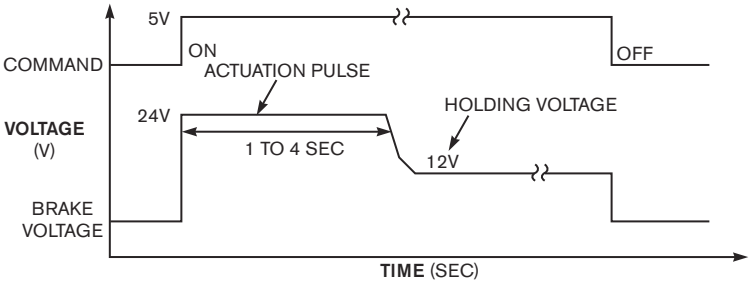

Figure 4 After the actuation pulse applies full voltage to the brake, the regulator's output gradually decreases to the nominal holding voltage.

Analog divider uses few components

David Cripe, Chatham, IL

Although microprocessors may offer more-precise calculations, there's still room for analog-computation techniques in a designer's circuit collection. As a case in point, the analog-divider circuit in **Figure 1** offers reasonably good accuracy for the price of a few inexpensive components. Given two voltages, V_A and V_B, as its inputs, the circuit delivers an output of 5V multiplied by the ratio of V_A divided by V_B. In operation, a TLC555, the CMOS version of the ubiquitous 555 timer, serves as a free-running Schmitt-trigger RC oscillator, IC_2. Its output signal at Pin 3 drives resistor R_1 and capacitor C_1. The voltage at C_1 drives IC_2's trigger (Pin 2) and threshold (Pin 6) inputs, closing the timing loop and establishing oscillation. A low-impedance open-drain MOSFET at IC_2's discharge pin switches low whenever IC_2's output goes low.

Representing the calculation's denominator, an input voltage, V_B, drives IC_2's discharge pin through a resistive-voltage divider comprising R_3 and R_4. Regardless of IC_2's frequency of oscillation, a pulsed voltage appears at IC_2's Pin 7 with the same duty cycle as IC_2's output signal at Pin 3 and an amplitude of 0V to $V_B/2$. A voltage follower, IC_{1B}, buffers IC_2's discharge output and drives a lowpass filter comprising R_8 and C_3, yielding a voltage that equals $V_B/2$ multiplied by IC_2's duty cycle. A second resistive voltage divider, R_6 and R_7, halves the numerator-input voltage, V_A, and applies the signal to integrator IC_{1A}, along with the output from the lowpass filter, R_8 and C_3. The integrator's output voltage drives current through R_2 into C_1, creating a bias voltage that in turn controls IC_2's output pulse width and forming a feedback loop.

In operation, the feedback loop forces IC_2's duty cycle to equalize the voltages at IC_{1A}'s Pin 2 and Pin 3, such that V_B multiplied by the duty cycle equals V_A, or the duty cycle equals the ratio of V_A to V_B. IC_2's output at Pin 3 comprises a 0 to 5V pulse waveform. The feedback circuit controls this waveform and in turn drives a lowpass filter, R_5 and C_4, to generate a dc-output

voltage equal to 5V multiplied by the pulse width, or $V_A \times 5V/V_B$.

Aside from the tolerances of the resistors in divider networks R_3 and R_4 and R_6 and R_7, the primary source for inaccuracy in the circuit arises from the nonzero on-resistance of IC_2's discharge switch and the inability of discharge-switch-voltage follower IC_{1A}'s output to reach 0V. Keeping the circuit's resistance values high tends to reduce this effect. A Spice simulation of this circuit indicates that, aside from the effects of resistor tolerances, the circuit achieves a worst-case accuracy of 0.5%. (Editor's note: For greatest accuracy, use a regulated, 5V power supply.) EDN

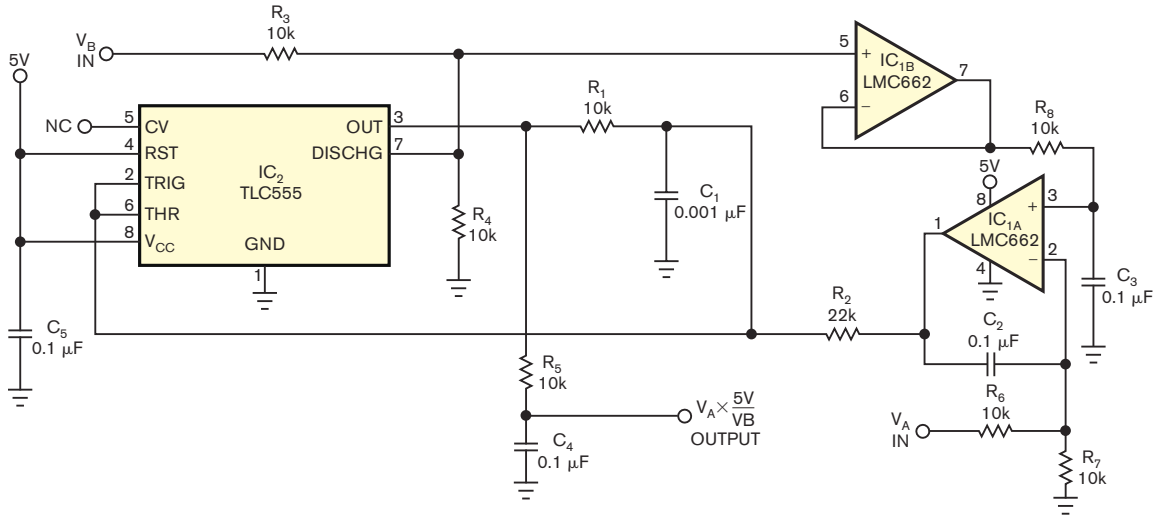

Figure 1 This low-cost pulse-width modulator performs analog division. Inputs V_A and V_B control this low-cost pulse-width modulator, and a lowpass filter follows it.

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Infineon Technologies, www.infineon.com

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On Semiconductor, www.onsemi.com

200V DirectFET MOSFET provides low typical on-resistance

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International Rectifier, www.irf.com

Miniature packaging provides high-current density

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Vishay, www.vishay.com

High-performance MOSFET suits low-voltage portable electronics

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Fairchild Semiconductor, www.fairchildsemi.com

Power MOSFET drives high currents at low voltage-gate threshold

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STMicroelectronics, www.st.com

productroundup

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Blade server combines dual-core processor and MCH

The CompactPCI blade server combines the 1.67-GHz dual-core Xeon processor with Intel's E7520-server-class MCH (memory-control hub). Providing scalability, the server includes as much as 4 Gbytes of DDR-2-400 SDRAM with dual Gigabit Ethernet ports on the backplane. Compliant with switched-backplane recommendation PICMG 2.16/VITA 31, the Ethernet ports also support the PICMG 2.9/VITA 38 IPMI (intelligent-platform-management interface). Additional features include two Gigabit Ethernet ports and two USB 2.0 ports on the front panel. A SATA port, two USB 2.0 ports, and a PCI Express port are also available on the back-panel connector as PICMG 2.16 dual Gigabit Ethernet interfaces. The cPENTXM2 costs $3950.
Thales, www.thalescomputers.com

PCI CPU card provides wireless support

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Mesa Electronics, www.mesanet.com

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LOOKING BACK

TO THE FIRST THOUGHTS OF DESKTOP COMPUTING

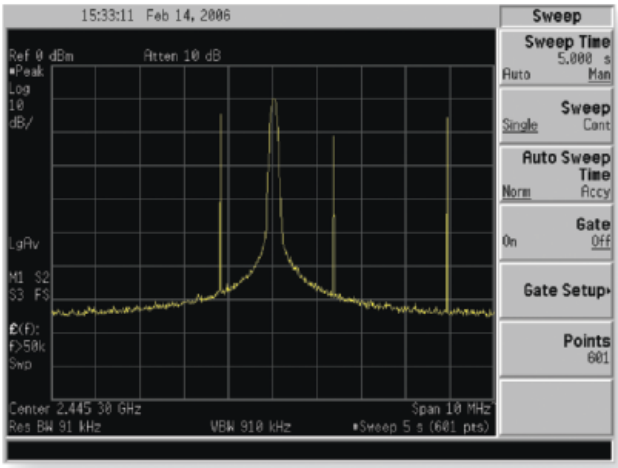
A low-priced, general-purpose computer featuring external programming is designed for problems too small for giant systems but too tedious for calculators. Compact, the system occupies less than half the surface of a desk. The key feature of the Burroughs Electro-Data E101 is an external pin-board program containing instructions to the computer, which may be changed quickly for different applications. Permanent program storage is provided by paper template overlays, which may be filed for future use. A 100- or 220-word internal magnetic-drum memory stores numeric information, with a word length of 12 decimal digits plus sign. Computational speeds are 20 additions or subtractions and four multiplications or divisions per second.

—*Electrical Design News*, January 1957

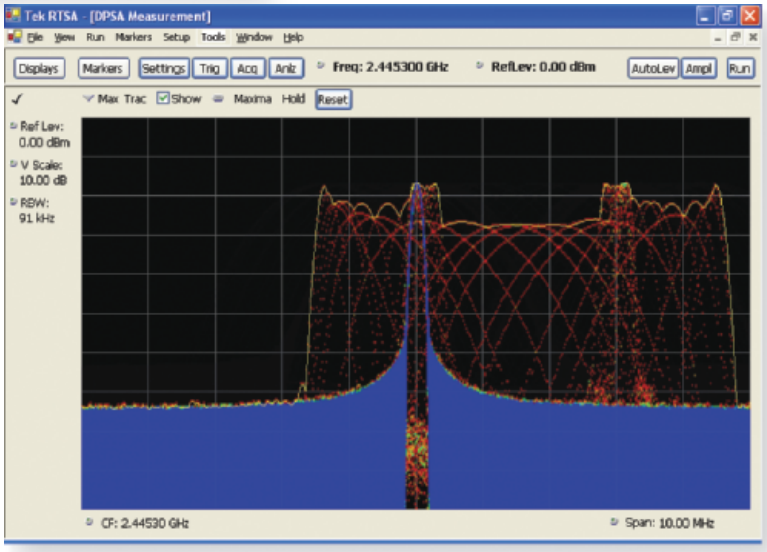
LOOKING AROUND

Is everyone going to CES?

You might think so, from the way the analysts are focusing on consumer electronics as the main driver for growth in electronics. But, as all those executives head hungrily to Las Vegas, it's worth remembering that growth in the consumer-electronics market comes with a whole list of conditions. It depends on consumers—especially in the United States—continuing to spend, even in the face of economic slowdown and rising mortgage defaults. It depends on Chinese manufacturers continuing to control costs, even in the face of labor shortages, growing social unrest, and upward pressure on the Chinese currency. And it depends on having well-executed designs and finding an audience—no longer a sure thing in light of recent horror stories from Sony, Nintendo, and Microsoft, to name a few. But we confidently march forward.



Agilent 5 seconds



Tektronix 5 seconds

The two screens represent an Agilent E4440A PSA and a Tektronix RSA6114A running DPX™, each detecting an identical signal that changes frequency every 1.28 seconds.

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Tektronix RSA6100A Series Real-Time Spectrum Analyzers. Nothing else comes close. Troubleshooting transient glitches? Use the best tool. One with greater capture bandwidth (110 MHz) than Agilent, uniquely combined with 73 dB spurious free dynamic range (SFDR) for complete analysis. And nearly 1000 times more spectrum measurements per second than existing products (48,000 spectrum measurements/sec vs. Agilent's 50). And an intuitive color display that shows a live view of your signal changing over time. You'll see RF signal characteristics that are practically invisible with any other instrument.

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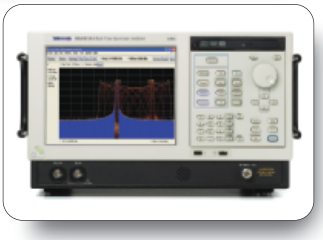

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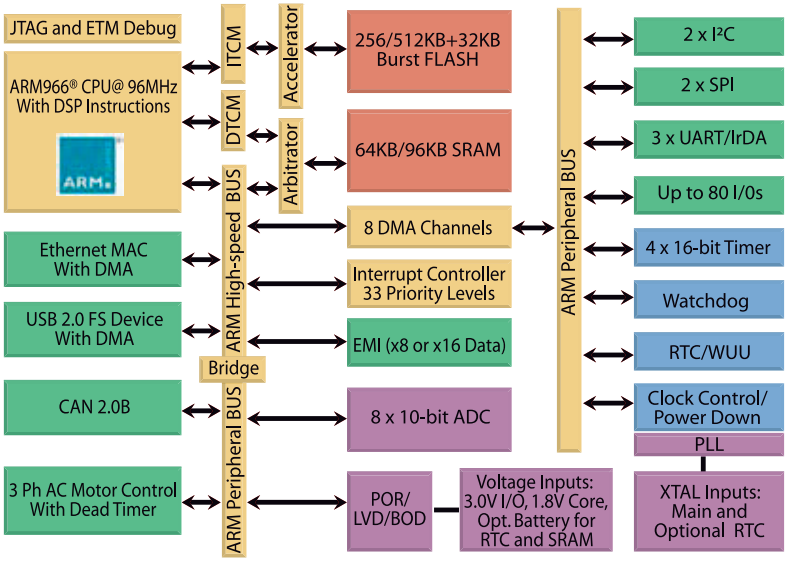

World's first ARM9-based general-purpose Flash microcontroller enables new generation of networked embedded applications

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Part Number	Flash Memory (KB)	RAM (KB)	A/D Inputs	Timer Functions		Serial Interface	GPIO (HI Current)	Package	Supply Voltage	Special Features
				(IC/OC/ PWM)	Other					
STR910FM32X	256 + 32	64	8x10-bit	7x16-bit (8,8,7)	RTC WDG	2xSPI 2xI²C 3xUART w/IrDA	40 (16)	LQFP80	Core: 1.8V I/O: 2.7 to 3.6V	CAN
STR910FW32X	256 + 32	64	8x10-bit				80 (16)	LQFP128		CAN, EMI
STR911FM42X	256 + 32	96	8x10-bit				40 (16)	LQFP80		USB, CAN
STR911FM44X	512 + 32	96	8x10-bit				40 (16)	LQFP80		USB, CAN
STR912FW42X	256 + 32	96	8x10-bit				80 (16)	LQFP128		Ethernet, USB, CAN, EMI
STR912FW44X	512 + 32	96	8x10-bit				80 (16)	LQFP128		Ethernet, USB, CAN, EMI

For further information, datasheets, and application notes, visit **www.st.com/str9**

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